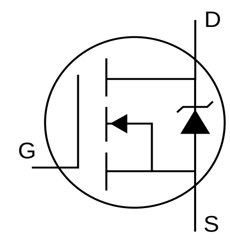
IRL2203NS/IRL2203NL

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 30V

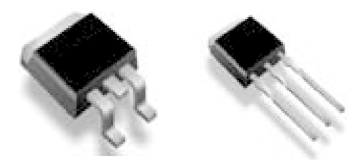
$R_{DS(on)}$ = 7.0mΩ

I_D = 116A⑦

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D^2Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D^2Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application. The through-hole version (IRL2203NL) is available for low-profile applications.



D^2Pak
IRL2203NS

TO-262
IRL2203NL

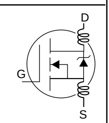
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	116⑦	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	82	
I_{DM}	Pulsed Drain Current ①	400	
P_D @T_A = 25°C	Power Dissipation	3.8	W
P_D @T_C = 25°C	Power Dissipation	180	W
	Linear Derating Factor	1.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
I_{AR}	Avalanche Current①	60	A
E_{AR}	Repetitive Avalanche Energy①	18	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

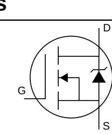
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	–––	0.85	°C/W
$R_{\theta JA}$	Junction-to-Ambient(PCB Mounted,steady-state)⑧	–––	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	–––	–––	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.029	–––	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	7.0	mΩ	V_{GS} = 10V, I_D = 60A ④
		–––	–––	10		V_{GS} = 4.5V, I_D = 48A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	–––	–––	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	73	–––	–––	S	V_{DS} = 25V, I_D = 60A④
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	25	µA	V_{DS} = 30V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -16V
Q_g	Total Gate Charge	–––	–––	60	nC	I_D = 60A
Q_{gs}	Gate-to-Source Charge	–––	–––	14		V_{DS} = 24V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	–––	33		V_{GS} = 4.5V, See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time	–––	11	–––		V_{DD} = 15V
t_r	Rise Time	–––	160	–––		I_D = 60A
$t_{d(off)}$	Turn-Off Delay Time	–––	23	–––		R_G = 1.8Ω
t_f	Fall Time	–––	66	–––		V_{GS} = 4.5V, See Fig. 10 ④
L_D	Internal Drain Inductance	–––	4.5	–––	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	–––	7.5	–––		
C_{iss}	Input Capacitance	–––	3290	–––		V_{GS} = 0V
C_{oss}	Output Capacitance	–––	1270	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	170	–––	pF	ƒ = 1.0MHz, See Fig. 5
E_{AS}	Single Pulse Avalanche Energy②	–––	1320⑤	290⑥	mJ	I_{AS} = 60A, L = 0.16mH

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	116⑦	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)①	–––	–––	400		
V_{SD}	Diode Forward Voltage	–––	–––	1.2	V	T_J = 25°C, I_S = 60A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	56	84	ns	T_J = 25°C, I_F = 60A
Q_{rr}	Reverse Recovery Charge	–––	110	170	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 0.16mH R_G = 25Ω, I_{AS} = 60A, V_{GS}=10V (See Figure 12)

③ $I_{SD} \le$ 60A, di/dt $\le$ 110A/µs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 175°C

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ This is a typical value at device destruction and represents operation outside rated limits.

⑥ This is a calculated value limited to T_J = 175°C .

⑦ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

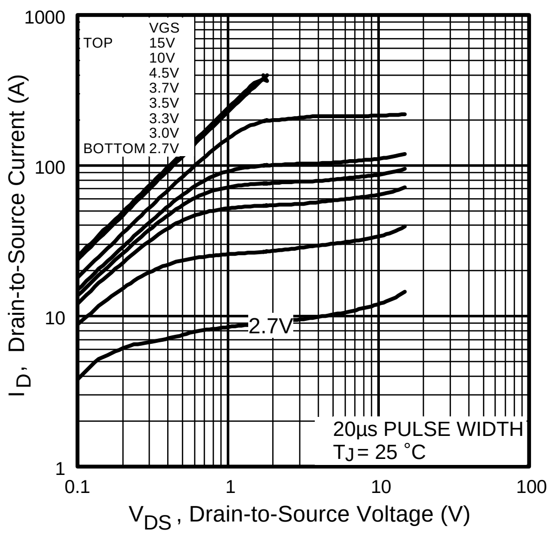


Fig 1. Typical Output Characteristics

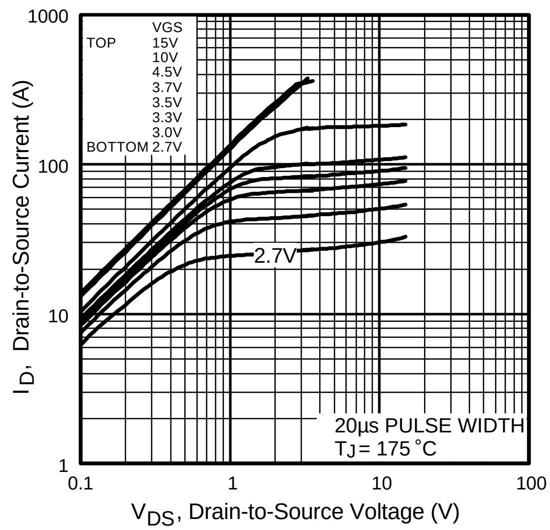


Fig 2. Typical Output Characteristics

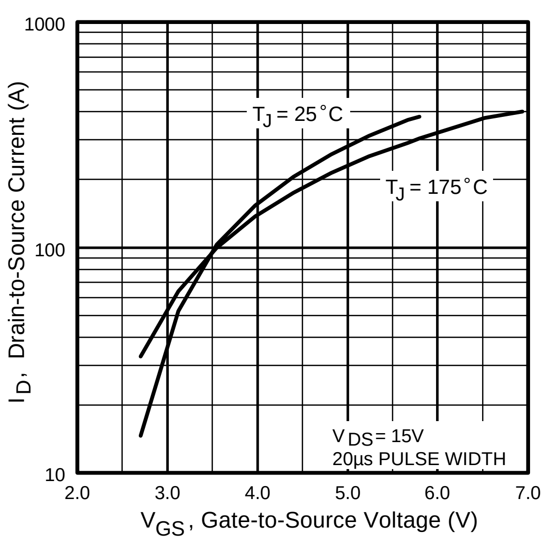


Fig 3. Typical Transfer Characteristics

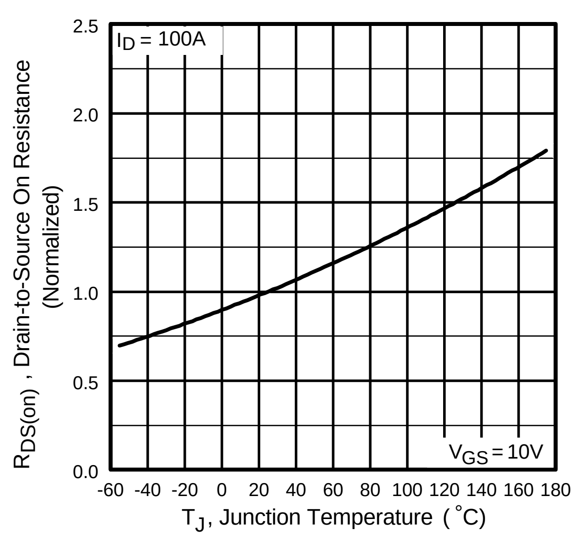


Fig 4. Normalized On-Resistance Vs. Temperature

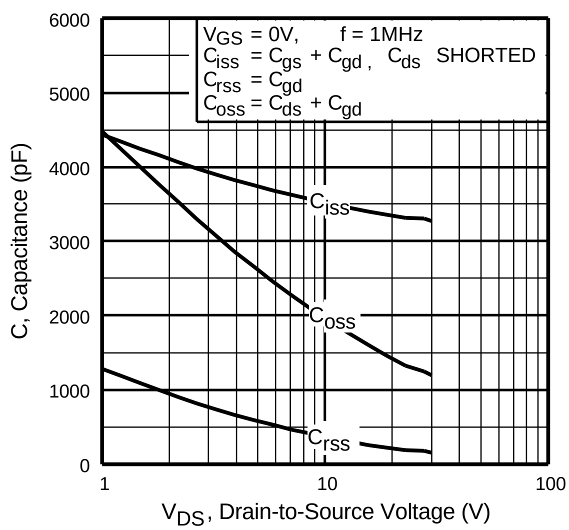


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

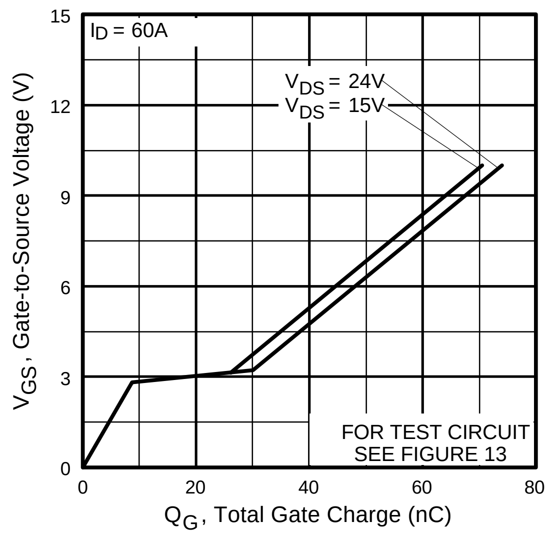


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

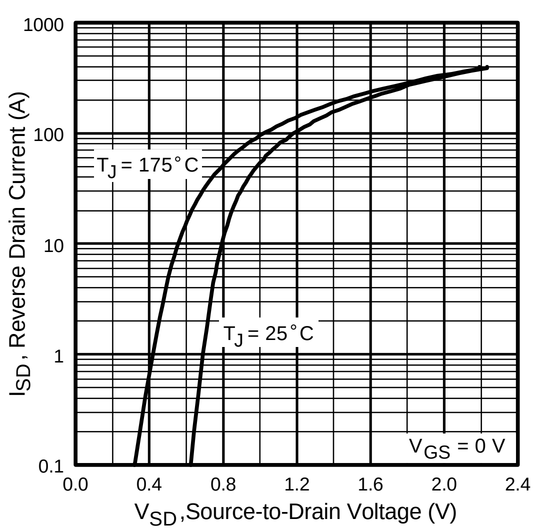


Fig 7. Typical Source-Drain Diode Forward Voltage

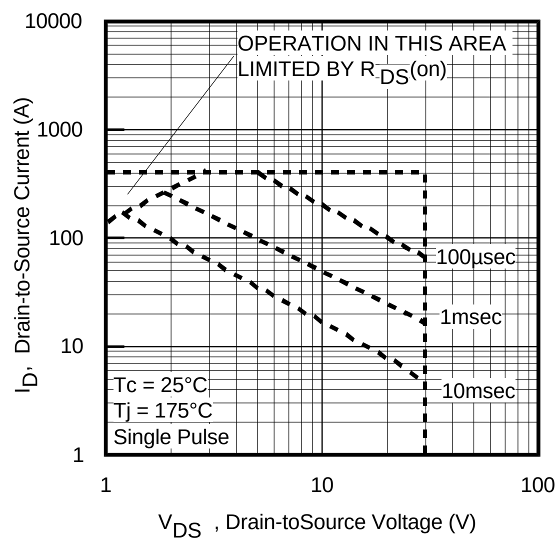


Fig 8. Maximum Safe Operating Area

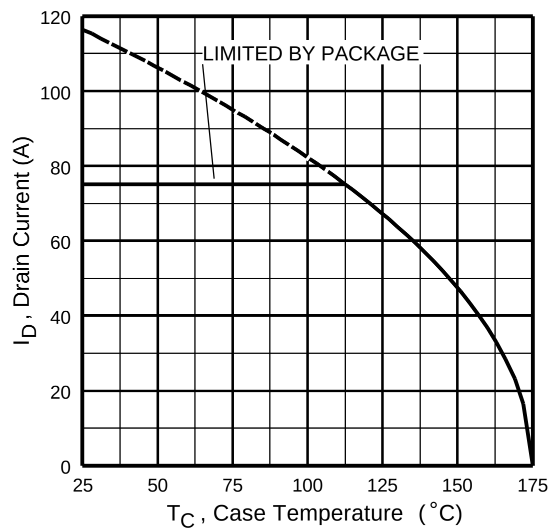


Fig 9. Maximum Drain Current Vs. Case Temperature

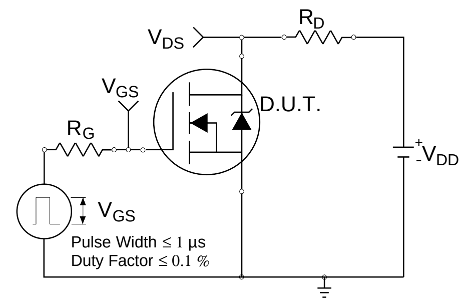


Fig 10a. Switching Time Test Circuit

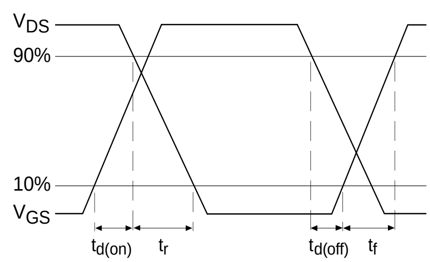


Fig 10b. Switching Time Waveforms

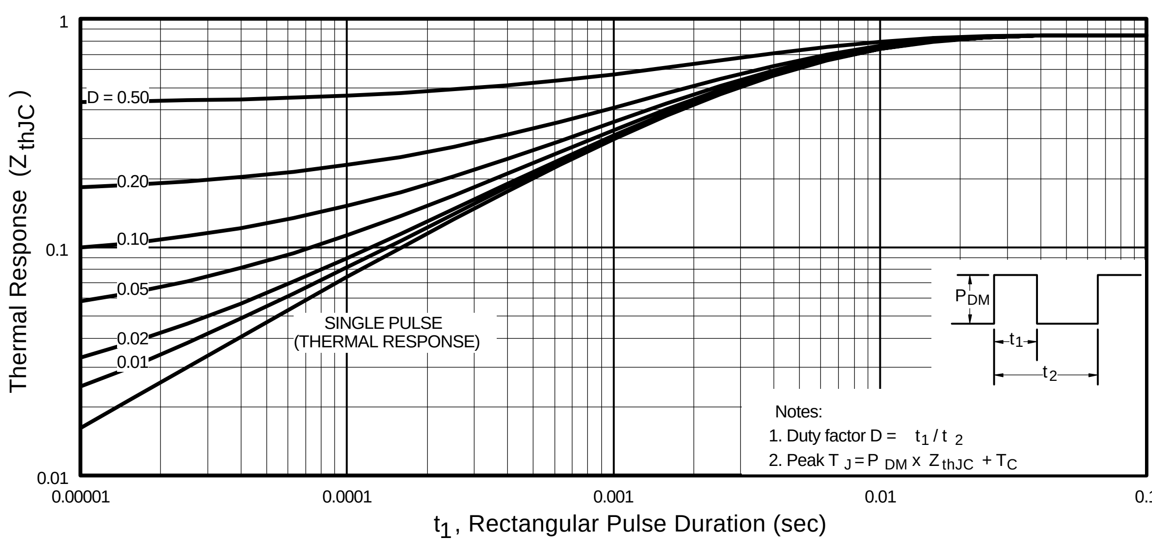


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

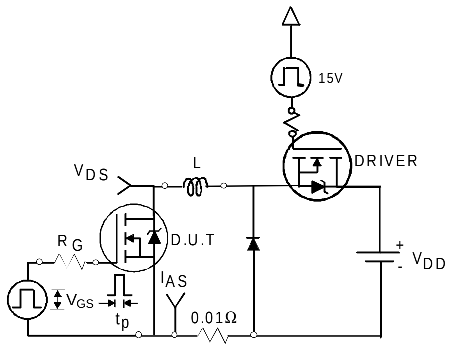


Fig 12a. Unclamped Inductive Test Circuit

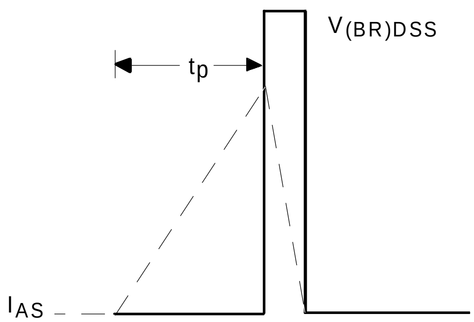


Fig 12b. Unclamped Inductive Waveforms

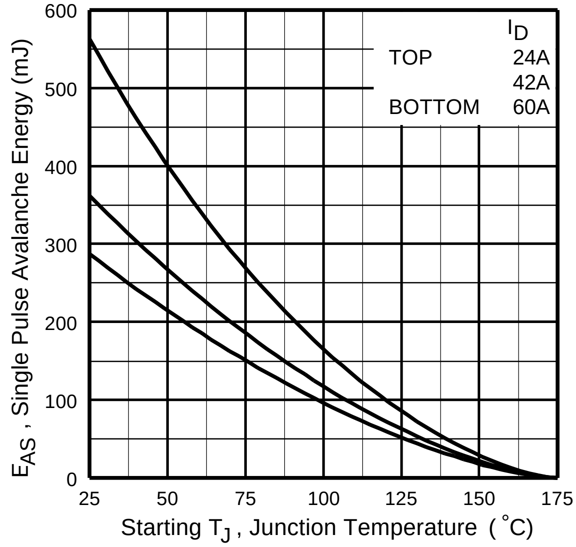


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

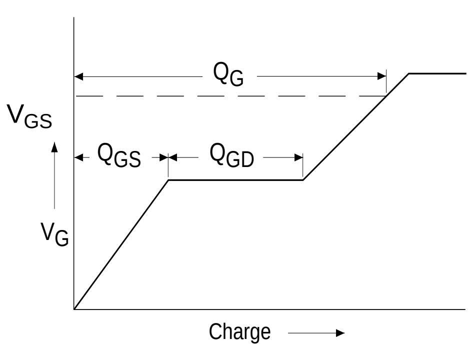


Fig 13a. Basic Gate Charge Waveform

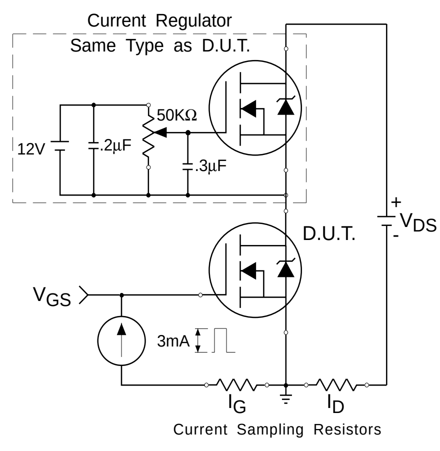
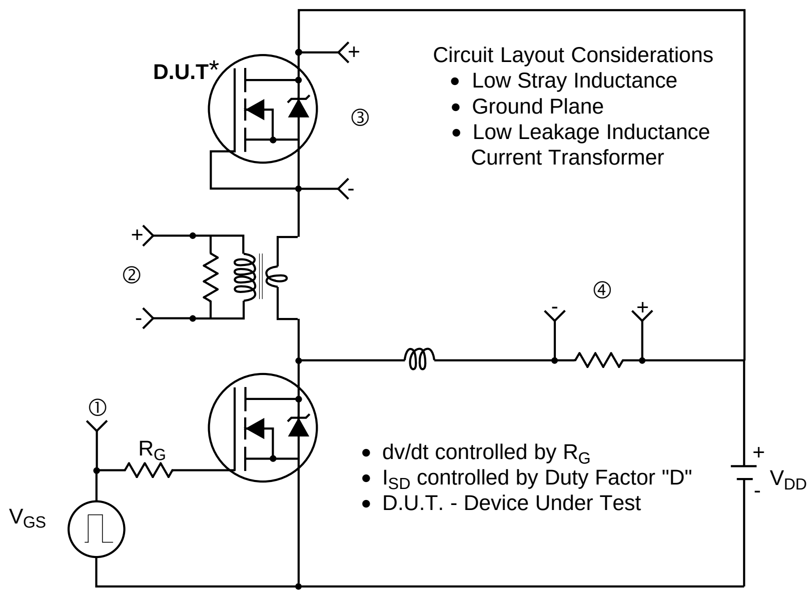
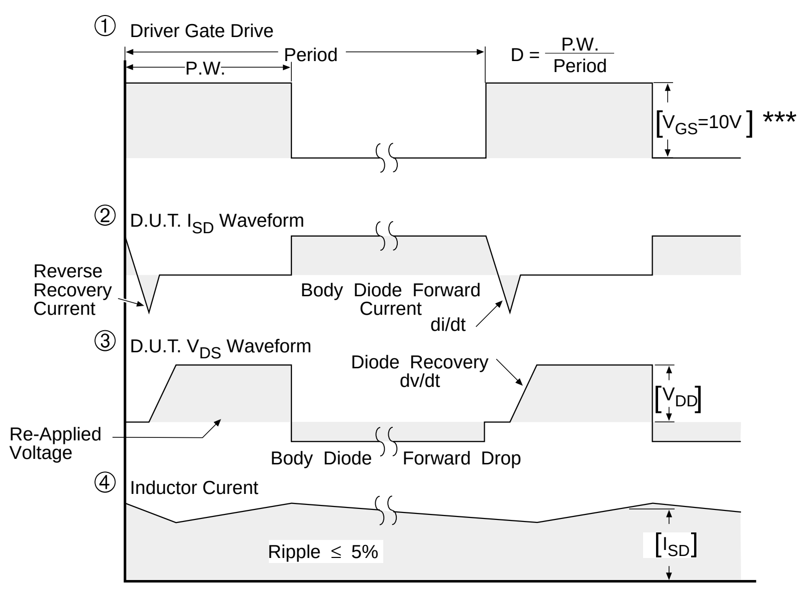


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



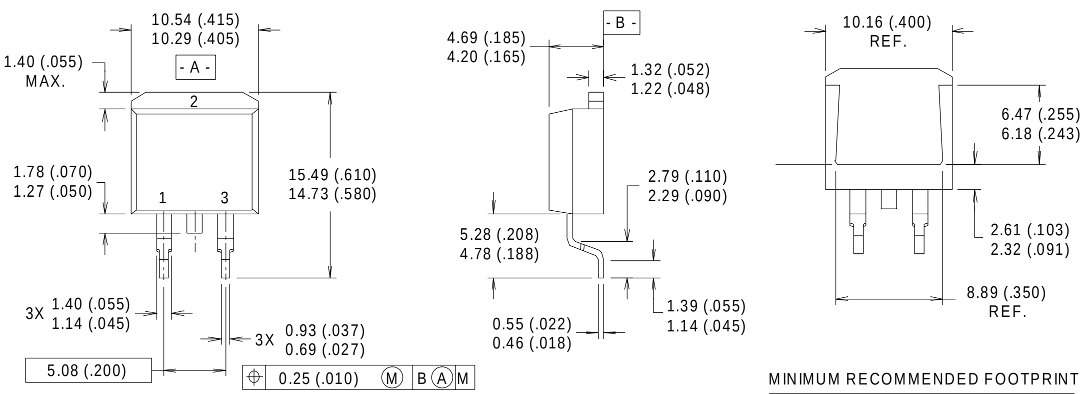
*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

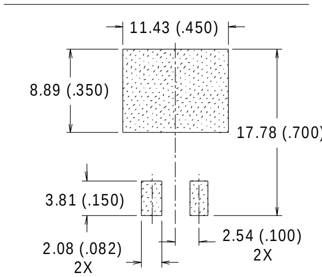
IRL2203NS/IRL2203NL

D²Pak Package Outline

Dimensions are shown in millimeters (inches)



MINIMUM RECOMMENDED FOOTPRINT



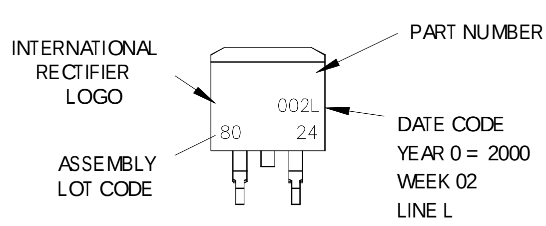
NOTES:

1. DIMENSIONS AFTER SOLDER DIP.
2. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION : INCH.
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE

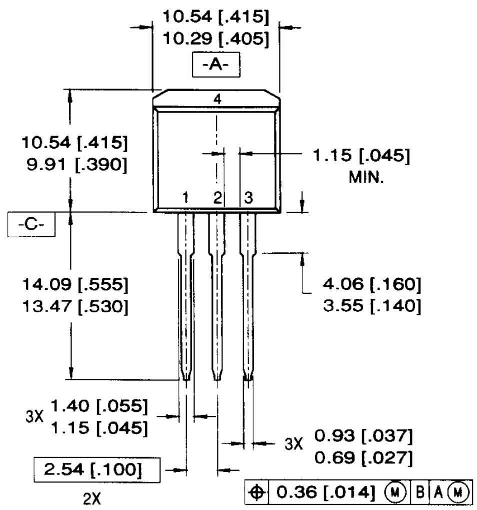
D²Pak Part Marking Information

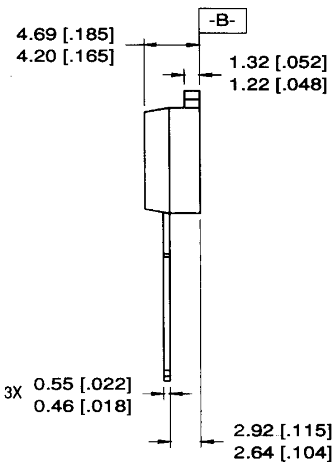
EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"



TO-262 Package Outline

Dimensions are shown in millimeters (inches)





LEAD ASSIGNMENTS

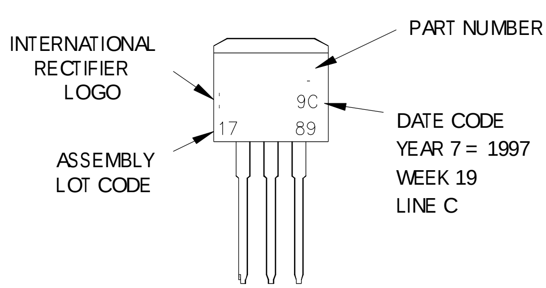
1 = GATE 3 = SOURCE
2 = DRAIN 4 = DRAIN

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

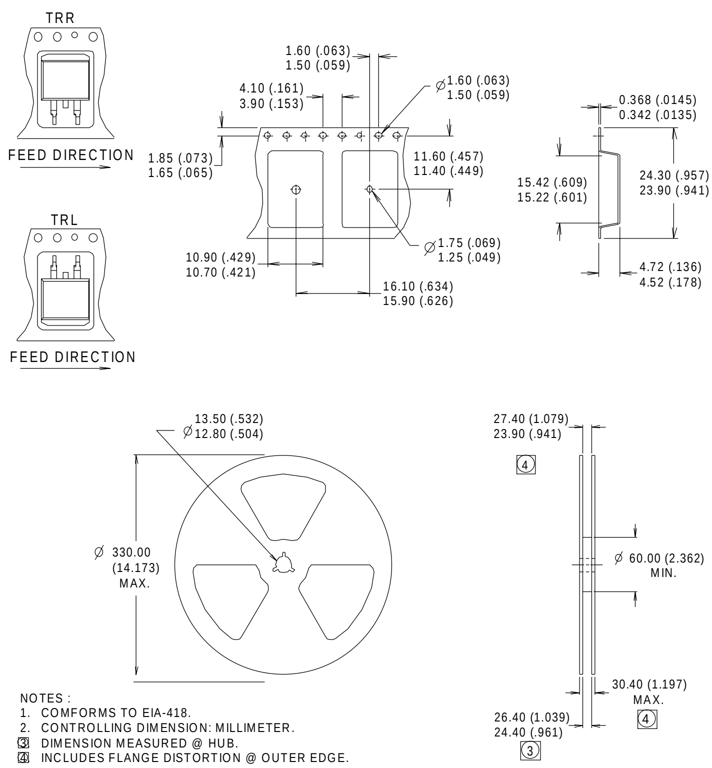
EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



IRL2203NS/IRL2203NL

D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.