STB20NK50Z, STF20NK50Z STP20NK50Z, STW20NK50Z

N-channel 500 V, 0.23 Ω, 17 A SuperMESH™ Power MOSFET Zener-protected TO-220, TO-247, TO-220FP, D^{2}PAK

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	P_W
STB20NK50Z	500 V	< 0.27 Ω	17 A	190 W
STF20NK50Z	500 V	< 0.27 Ω	17 A	40 W
STP20NK50Z	500 V	< 0.27 Ω	17 A	190 W
STW20NK50Z	500 V	< 0.27 Ω	17 A	190 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability

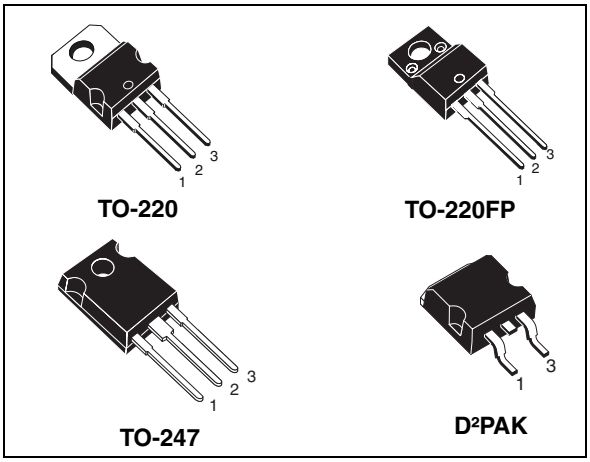
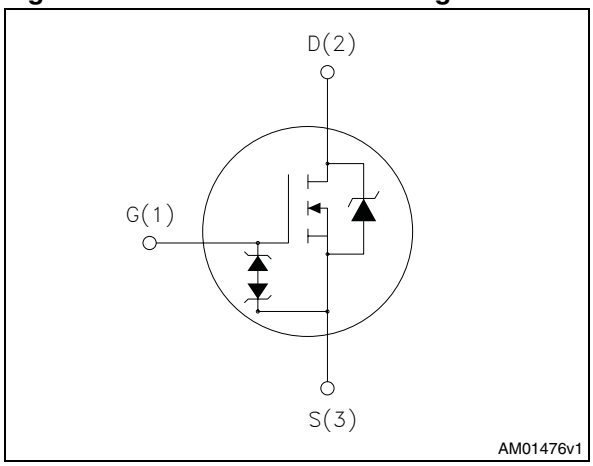


Figure 1. Internal schematic diagram



Application

- Switching applications

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB20NK50Z	B20NK50Z	D²PAK	Tape and reel
STF20NK50Z	F20NK50Z	TO-220FP	Tube
STP20NK50Z	P20NK50Z	TO-220	
STW20NK50Z	W20NK50Z	TO-247	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, TO-247, D²PAK	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	500		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25 °C	17	17(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	10.71	10.71	A
I_{DM} (2)	Drain current (pulsed)	68	68	A
P_{TOT}	Total dissipation at T_C = 25 °C	190	40	W
	Derating factor	1.51		W/°C
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	--	2500	V
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100 pF, R=1.5 kΩ)	6000		
dv/dt (3)	Peak diode recovery voltage slope	4.5		V/ns
T_{stg}	Storage temperature	-55 to 150		°C
T_j	Max operating junction temperature	150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 17$ A, di/dt $\leq$ 200 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220, D²PAK	TO-247	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	0.66		3.1	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	50	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300			°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	17	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=I_{AR}, V_{DD}=50 V)	850	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D =1 mA, V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 8.5 A		0.23	0.27	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 8.5 A	-	13		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	2600 328 72		pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{DS} =0, V_{DS} = 0 to 640 V	-	187		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 250 V, I_D = 8.5 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	28 20 70 15		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 400 V, I_D = 17 A, V_{GS} = 10 V	-	85 15.5 42	119	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)		-		17 68	A A
V_{SD}(2)	Forward on voltage	I_{SD} = 17 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 17 A, di/dt = 100 A/µs V_R = 100 V	-	355 3.90 22		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 17 A, di/dt = 100 A/µs V_R = 100 V, Tj = 150 °C	-	440 5.72 26		ns µC A

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. Pulse width limited by safe operating area

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1mA (open drain)	30			V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.