



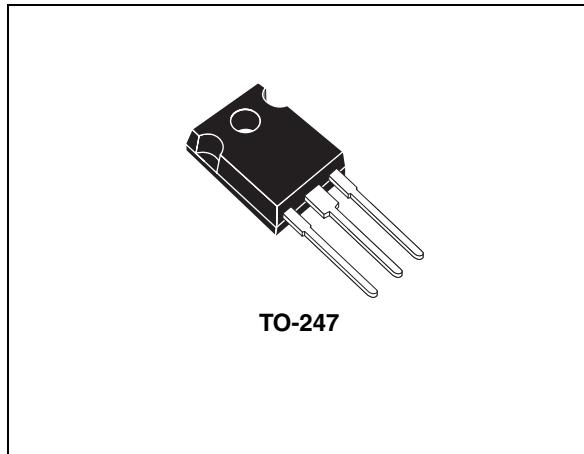
STW13NK100Z

N-channel 1000V - 0.56Ω - 13A - TO-247
Zener - Protected SuperMESH™ PowerMOSFET

General features

Type	V _{DSS} (@T _{jmax})	R _{DS(on)}	I _D	P _W
STW13NK100Z	1000 V	< 0.70 Ω	13 A	350W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



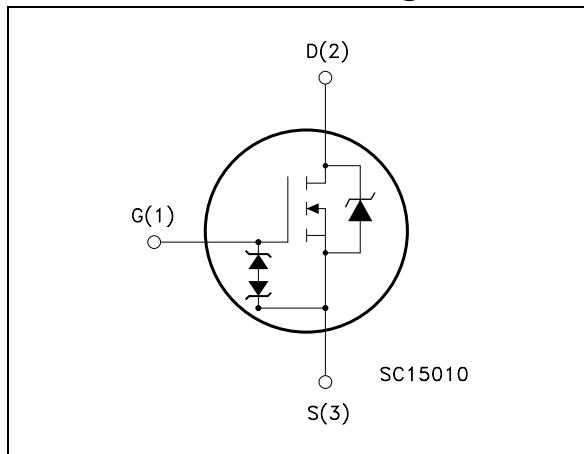
Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STW13NK100Z	W13NK100Z	TO-247	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	1000	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20K\Omega$)	1000	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25^\circ C$	13	A
I_D	Drain current (continuous) at $T_C=100^\circ C$	8.2	A
$I_{DM}^{(1)}$	Drain current (pulsed)	52	A
P_{TOT}	Total dissipation at $T_C = 25^\circ C$	350	W
	Derating Factor	2.7	W/ $^\circ C$
$V_{ESD} (G-S)$	Gate source ESD(HBM-C=100pF, R=1,5K Ω)	6000	V
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ C$

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 8.3$ A, $dI/dt \leq 200A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	0.36	$^\circ C/W$
R_{thj-a}	Thermal resistance junction-ambient Max	50	$^\circ C/W$
T_I	Maximum lead temperature for soldering purpose	300	$^\circ C$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max)	13	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25^\circ C$, $I_d=I_{ar}$, $V_{dd}=50V$)	700	mJ

Table 4. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	$I_{GS}=\pm 1\text{mA}$ (Open Drain)	30			V

2 Electrical characteristics

($T_{CASE}=25^\circ\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{mA}$, $V_{GS} = 0$	1000			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating}$, $T_c = 125^\circ\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{GS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 10	μA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 150\ \mu\text{A}$	3	3.75	4.5	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 6.5\ \text{A}$		0.56	0.70	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$, $I_D = 6.5\ \text{A}$		14		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$		6000 455 100		pF pF pF
$C_{osseq}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{V}$ to 800V		227		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Off-voltage rise time Fall time	$V_{DD} = 500\ \text{V}$, $I_D = 7\ \text{A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{V}$		45 35 145 45		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 800\text{V}$, $I_D = 13\ \text{A}$ $V_{GS} = 10\text{V}$		190 30 100	266	nC nC nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				13	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				52	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=8.3A, V_{GS}=0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=13\text{ A},$ $di/dt = 100\text{A}/\mu\text{s},$ $V_{DD}=100\text{ V}, T_j=25^\circ\text{C}$		820 12.7 31		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=13\text{ A},$ $di/dt = 100\text{A}/\mu\text{s},$ $V_{DD}=100\text{V}, T_j=150^\circ\text{C}$		1050 17.8 34		ns μC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%