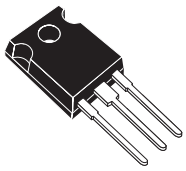
STW11NK90Z

N-channel 900V - 0.82Ω - 9.2A - TO-247
Zener-protected SuperMESH™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STW11NK90Z	900V	<0.98Ω	9.2A	200W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeability



TO-247

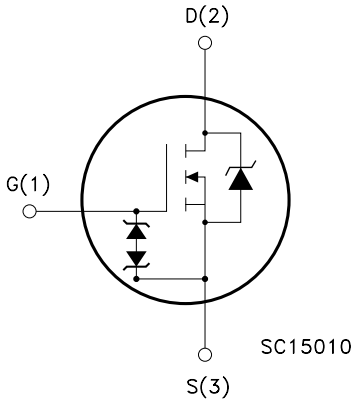
Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage Power MOSFETs including revolutionary MDmesh™ products

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STW11NK90Z	W11NK90Z	TO-247	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	900	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	900	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25°C	9.2	A
I_D	Drain current (continuous) at T_C=100°C	5.8	A
I_{DM}(1)	Drain current (pulsed)	36.8	A
P_{TOT}	Total dissipation at T_C = 25°C	200	W
	Derating factor	1.51	W/°C
$V_{ESD(G-D)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	6000	V
dv/dt(2)	Peak diode recovery voltage slope	4.5	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq$ 9.2A, di/dt $\leq$ 200A/µs, V_{DD} =80%$V_{(BR)DSS}$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	0.66	°C/W
R_{thj-a}	Thermal resistance junction-ambient Max	50	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	9.2	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	400	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS}= 0	900			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125°C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 100µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 4.6A		0.82	0.98	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =15V, I_D = 4.6A		11		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		3000 240 48		pF pF pF
$C_{oss\ eq}$(2).	Equivalent output capacitance	V_{GS}=0, V_{DS} =0V to 720V		83		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=720V, I_D = 9.2A V_{GS} =10V		95 14 49	115	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} inceases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}=450 V, I_D= 4.6A, R_G=4.7Ω, V_{GS}=10V		30 19 76 50		ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				9.2	A
I_{SDM}(1)	Source-drain current (pulsed)				36.8	A
V_{SD}(2)	Forward on voltage	I_{SD}=9.2A, V_{GS}=0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=9.2A, di/dt = 100A/µs, V_{DD}=50V, Tj=25°C		584 6 21		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=9.2A, di/dt = 100A/µs, V_{DD}=50V, Tj=150°C		790 8.7 22		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 8. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}(1)	Gate-source breakdown voltage	Igs=±1mA (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.