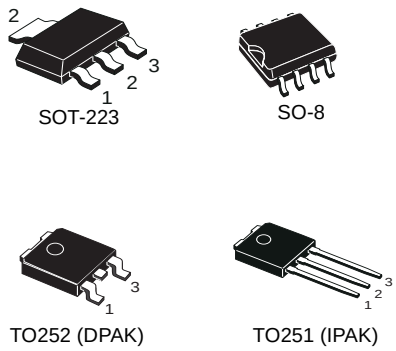
VNN7NV04, VNS7NV04
VND7NV04, VND7NV04-1

OMNIFET II
fully autoprotected Power MOSFET

Features

Type	$R_{DS(on)}$	I_{lim}	V_{clamp}
VNN7NV04 VNS7NV04 VND7NV04 VND7NV04-1	60 mΩ	6 A	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET in compliance with the 2002/95/EC European Directive



Description

The VNN7NV04, VNS7NV04, VND7NV04 VND7NV04-1, are monolithic devices designed in STMicroelectronics VIPower M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 50 kHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

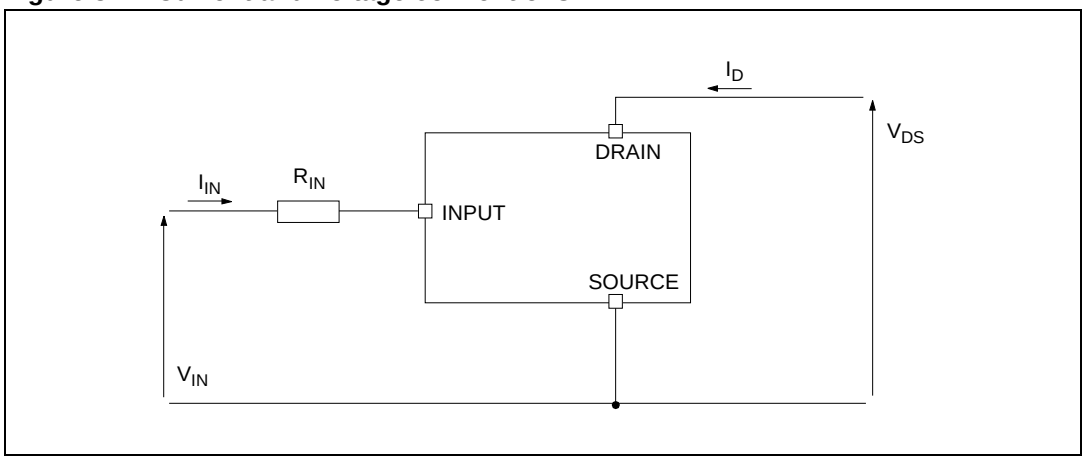
Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Package	Order codes			
	Tube	Tube (lead-free)	Tape and reel	Tape and reel (lead-free)
SOT-223	VNN7NV04	-	VNN7NV0413TR	-
SO-8	VNS7NV04	-	VNS7NV0413TR	-
TO-252	VND7NV04	VND7NV04-E	VND7NV0413TR	VND7NV04TR-E
TO-251	VND7NV04-1	VND7NV04-1-E	-	-

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		SOT-223	SO-8	DPAK/IPAK	
V_{DS}	Drain-source voltage (V_{IN}=0 V)	Internally clamped			V
V_{IN}	Input voltage	Internally clamped			V
I_{IN}	Input current	+/-20			mA
$R_{IN\ MIN}$	Minimum input series impedance	150			Ω
I_D	Drain current	Internally limited			A
I_R	Reverse DC output current	-10.5			A
V_{ESD1}	Electrostatic discharge (R=1.5 KΩ, C=100 pF)	4000			V
V_{ESD2}	Electrostatic discharge on output pin only (R=330 Ω, C=150 pF)	16500			V
P_{tot}	Total dissipation at T_c=25 °C	7	4.6	60	W
E_{MAX}	Maximum switching energy (L=0.7 mH; R_L=0 Ω; V_{bat}=13.5 V; T_{jstart}=150 ºC; I_L=9 A)	40		40	mJ
E_{MAX}	Maximum switching energy (L=0.6 mH; R_L=0 Ω; V_{bat}=13.5 V; T_{jstart}=150 ºC; I_L=9 A)		37		mJ
T_j	Operating junction temperature	Internally limited			°C
T_c	Case operating temperature	Internally limited			°C
T_{stg}	Storage temperature	-55 to 150			°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		SOT-223	SO-8	DPAK	IPAK	
$R_{thj-case}$	Thermal resistance junction-case max	18		2.1	2.1	°C/W
$R_{thj-lead}$	Thermal resistance junction-lead max		27			°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	96(1)	90(1)	65(1)	102	°C/W

1. When mounted on a standard single-sided FR4 board with 0.5 mm^2 of Cu (at least 35 µm thick) connected to all DRAIN pins.

2.3 Electrical characteristics

-40 °C < T_j < 150 °C, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Off						
V_{CLAMP}	Drain-source clamp voltage	V_{IN}=0 V; I_D=3.5 A	40	45	55	V
V_{CLTH}	Drain-source clamp threshold voltage	V_{IN}=0 V; I_D=2 mA	36			V
V_{INTH}	Input threshold voltage	V_{DS}=V_{IN}; I_D=1 mA	0.5		2.5	V
I_{ISS}	Supply current from input pin	V_{DS}=0 V; V_{IN}=5 V		100	150	µA
V_{INCL}	Input-source clamp voltage	I_{IN}=1 mA I_{IN}=-1 mA	6 -1.0	6.8	8 -0.3	V
I_{DSS}	Zero input voltage drain current (V_{IN}=0 V)	V_{DS}=13 V; V_{IN}=0 V; T_j=25 °C V_{DS}=25 V; V_{IN}=0 V			30 75	µA
On						
$R_{DS(on)}$	Static drain-source on resistance	V_{IN}=5 V; I_D=3.5 A; T_j=25 °C V_{IN}=5 V; I_D=3.5 A			60 120	mΩ
Dynamic (T_j=25 °C, unless otherwise specified)						
g_{fs} (1)	Forward transconductance	V_{DD}=13 V; I_D=3.5 A		9		S
C_{OSS}	Output capacitance	V_{DS}=13 V; f=1 MHz; V_{IN}=0 V		220		pF

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Switching (T_j=25 °C, unless otherwise specified)						
$t_{d(on)}$	Turn-on delay time	V_{DD}=15 V; I_D=3.5 A V_{gen}=5 V; R_{gen}=$R_{IN\ MIN}$=150 Ω		100	300	ns
t_r	Rise time			470	1500	ns
$t_{d(off)}$	Turn-off delay time			500	1500	ns
t_f	Fall time			350	1000	ns
$t_{d(on)}$	Turn-on delay time	V_{DD}=15 V; I_D=3.5 A V_{gen}=5 V; R_{gen}=2.2 KΩ		0.75	2.3	µs
t_r	Rise time			4.6	14.0	µs
$t_{d(off)}$	Turn-off delay time			5.4	16.0	µs
t_f	Fall time			3.6	11.0	µs
$(dI/dt)_{on}$	Turn-on current slope	V_{DD}=15 V; I_D=3.5 A V_{gen}=5 V; R_{gen}=$R_{IN\ MIN}$=150 Ω		6.5		A/µs
Q_i	Total input charge	V_{DD}=12 V; I_D=3.5 A; V_{IN}=5 V I_{gen}=2.13 mA (see figure		18		nC
Source drain diode (T_j=25 °C, unless otherwise specified)						
V_{SD}(1)	Forward on voltage	I_{SD}=3.5 A; V_{IN}=0 V		0.8		V
t_{rr}	Reverse recovery time	I_{SD}=3.5 A; dI/dt=20 A/µs V_{DD}=30 V; L=200 µH		220		ns
Q_{rr}	Reverse recovery charge			0.28		µC
I_{RRM}	Reverse recovery current			2.5		A
Protections (-40 °C < T_j < 150 °C, unless otherwise specified)						
I_{lim}	Drain current limit	V_{IN}=5 V; V_{DS}=13 V	6	9	12	A
t_{dlim}	Step response current limit	V_{IN}=5 V; V_{DS}=13 V		4.0		µs
T_{jsh}	Over temperature shutdown		150	175	200	°C
T_{jrs}	Over temperature reset		135			°C
I_{gf}	Fault sink current	V_{IN}=5 V; V_{DS}=13 V; T_j=T_{jsh}		15		mA
E_{as}	Single pulse avalanche energy	starting T_j=25 °C; V_{DD}=24 V V_{IN}=5 V R_{gen}=$R_{IN\ MIN}$=150 Ω; L=24 mH	200			mJ

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %