

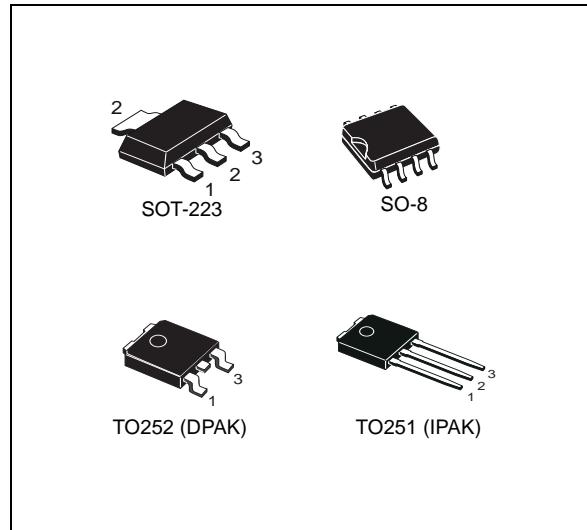
VNN3NV04, VNS3NV04 VND3NV04, VND3NV04-1

OMNIFET II
fully autoprotected Power MOSFET

Features

| Type | R _{DS(on)} | I _{lim} | V _{clamp} |
|------------|---------------------|------------------|--------------------|
| VNN3NV04 | | | |
| VNS3NV04 | 120 mΩ | 3.5 A | 40 V |
| VND3NV04 | | | |
| VND3NV04-1 | | | |

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET in compliance with the 2002/95/EC European Directive



Description

The VNN3NV04, VNS3NV04, VND3NV04, VND3NV04-1, are monolithic devices designed in STMicroelectronics™ VIPower™ M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 50 kHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

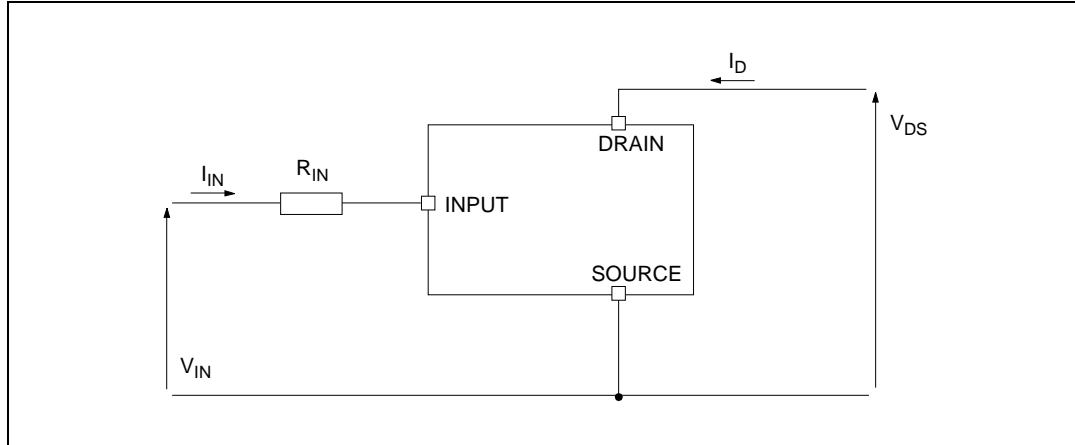
Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

| Package | Order codes | | | |
|---------|-------------|------------------|---------------|---------------------------|
| | Tube | Tube (lead-free) | Tape and reel | Tape and reel (lead-free) |
| SOT-223 | VNN3NV04 | - | VNN3NV0413TR | - |
| SO-8 | VNS3NV04 | - | VNS3NV0413TR | - |
| TO-252 | VND3NV04 | VND3NV04-E | VND3NV0413TR | VND3NV04TR-E |
| TO-251 | VND3NV04-1 | VND3NV04-1-E | - | - |

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | | | Unit |
|---------------|---|--------------------|------|-----------|----------|
| | | SOT-223 | SO-8 | DPAK/IPAK | |
| V_{DS} | Drain-source voltage ($V_{IN}=0$ V) | Internally clamped | | | V |
| V_{IN} | Input voltage | Internally clamped | | | V |
| I_{IN} | Input current | +/-20 | | | mA |
| $R_{IN\ MIN}$ | Minimum input series impedance | 220 | | | Ω |
| I_D | Drain current | Internally limited | | | A |
| I_R | Reverse DC output current | -5.5 | | | A |
| V_{ESD1} | Electrostatic discharge ($R=1.5$ K Ω , $C=100$ pF) | 4000 | | | V |
| V_{ESD2} | Electrostatic discharge on output pin only ($R=330$ Ω , $C=150$ pF) | 16500 | | | V |
| P_{tot} | Total dissipation at $T_c=25$ °C | 7 | 8.3 | 35 | W |
| T_j | Operating junction temperature | Internally limited | | | °C |
| T_c | Case operating temperature | Internally limited | | | °C |
| T_{stg} | Storage temperature | -55 to 150 | | | °C |

2.2 Thermal data

Table 3. Thermal data

| Symbol | Parameter | Value | | | | Unit |
|-----------------------|---|-------------------|-------------------|-------------------|------|------|
| | | SOT-223 | SO-8 | DPAK | IPAK | |
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 18 | | 3.5 | 3.5 | °C/W |
| $R_{thj\text{-}lead}$ | Thermal resistance junction-lead max | | 15 | | | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient max | 70 ⁽¹⁾ | 65 ⁽¹⁾ | 54 ⁽¹⁾ | 100 | °C/W |

- When mounted on a standard single-sided FR4 board with 50 mm^2 of Cu (at least 35 mm thick) connected to all DRAIN pins.

2.3 Electrical characteristics

-40 °C < T_i < 150 °C, unless otherwise specified.

Table 4. Electrical characteristics

Table 4. Electrical characteristics (continued)

| Symbol | Parameter | Test conditions | Min | Typ | Max | Unit |
|--|-------------------------------|---|-----|------|------|------------------------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}=15 \text{ V}; I_D=1.5 \text{ A}$ $V_{gen}=5 \text{ V}; R_{gen}=R_{IN \text{ MIN}}=220 \Omega$ | | 90 | 300 | ns |
| t_r | Rise time | | | 250 | 750 | ns |
| $t_{d(off)}$ | Turn-off delay time | | | 450 | 1350 | ns |
| t_f | Fall time | | | 250 | 750 | ns |
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}=15 \text{ V}; I_D=1.5 \text{ A}$ $V_{gen}=5 \text{ V}; R_{gen}=2.2 \text{ k}\Omega$ | | 0.45 | 1.35 | μs |
| t_r | Rise time | | | 2.5 | 7.5 | μs |
| $t_{d(off)}$ | Turn-off delay time | | | 3.3 | 10.0 | μs |
| t_f | Fall time | | | 2.0 | 6.0 | μs |
| $(dl/dt)_{on}$ | Turn-on current slope | $V_{DD}=15 \text{ V}; I_D=1.5 \text{ A}$ $V_{gen}=5 \text{ V}; R_{gen}=R_{IN \text{ MIN}}=220 \Omega$ | | 4.7 | | $\text{A}/\mu\text{s}$ |
| Q_i | Total input charge | $V_{DD}=12 \text{ V}; I_D=1.5 \text{ A}; V_{IN}=5 \text{ V}$ $I_{gen}=2.13 \text{ mA} \text{ (see figure)}$ | | 8.5 | | nC |
| Source drain diode ($T_j=25^\circ\text{C}$, unless otherwise specified) | | | | | | |
| $V_{SD}^{(1)}$ | Forward on voltage | $I_{SD}=1.5 \text{ A}; V_{IN}=0 \text{ V}$ | | 0.8 | | V |
| t_{rr} | Reverse recovery time | $I_{SD}=1.5 \text{ A}; dl/dt=12 \text{ A}/\mu\text{s}$ $V_{DD}=30 \text{ V}; L=200 \mu\text{H}$ | | 107 | | ns |
| Q_{rr} | Reverse recovery charge | | | 37 | | μC |
| I_{RRM} | Reverse recovery current | | | 0.7 | | A |
| Protections (-40 $^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified) | | | | | | |
| I_{lim} | Drain current limit | $V_{IN}=5 \text{ V}; V_{DS}=13 \text{ V}$ | 3.5 | 5 | 7 | A |
| t_{dlim} | Step response current limit | $V_{IN}=5 \text{ V}; V_{DS}=13 \text{ V}$ | | 10 | | μs |
| T_{jsh} | Over temperature shutdown | | 150 | 175 | 200 | $^\circ\text{C}$ |
| T_{jrs} | Over temperature reset | | 135 | | | $^\circ\text{C}$ |
| I_{gf} | Fault sink current | $V_{IN}=5 \text{ V}; V_{DS}=13 \text{ V}; T_j=T_{jsh}$ | 10 | 15 | 20 | mA |
| E_{as} | Single pulse avalanche energy | starting $T_j=25^\circ\text{C}; V_{DD}=24 \text{ V}$ $V_{IN}=5 \text{ V} R_{gen}=R_{IN \text{ MIN}}=220 \Omega; L=24 \text{ mH}$ | 100 | | | mJ |

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %