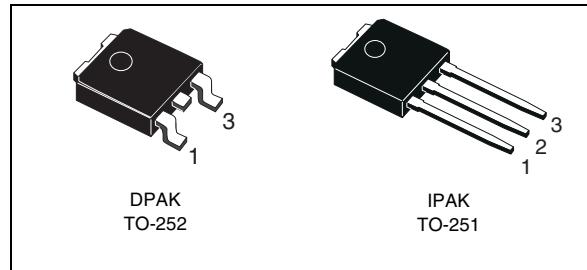


Features

Max on-state resistance (per ch.)	$R_{DS(on)}$	0.3Ω
Current limitation (typ)	I_{lim}	10A
Drain-Source clamp voltage	V_{CLAMP}	60V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Logic level input threshold
- ESD protection
- Schmitt trigger on input
- High noise immunity



Description

The VND10N06 and VND10N06-1 are monolithic devices designed in STMicroelectronics VIPower M0-2 technology, intended for replacement of standard Power MOSFETs in DC to 50KHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
DPAK	VND10N06	VND10N06TR
IPAK	VND10N06-1	

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSn}	Drain-Source voltage ($V_{in} = 0V$)	Internally clamped	V
V_{INn}	Input voltage	Internally clamped	V
I_{in}	Input current	± 20	mA
I_{Dn}	Drain current	Internally limited	A
I_{Rn}	Reverse DC output current	- 15	A
V_{ESD}	Electrostatic discharge ($R = 1.5K\Omega$ $C = 100pF$)	4000	V
P_{tot}	Total dissipation at $T_c = 25^\circ C$	35	W
T_j	Operating junction temperature	Internally limited	$^\circ C$
T_c	Case operating temperature	Internally limited	$^\circ C$
T_{stg}	Storage temperature	- 55 to 150	$^\circ C$

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj-case}$	Thermal resistance junction-case	3.5	$^\circ C/W$
$R_{thj-amb}$	Thermal resistance junction-ambient	100	$^\circ C/W$

2.3 Electrical characteristics

T_{case} = 25 °C unless otherwise stated.

Table 4. Off

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CLAMP}	Drain-Source clamp voltage	V _{IN} = 0V; I _D = 200mA	50	60	70	V
V _{IL}	Input low level voltage	I _D = 100 μA; V _{DS} = 16 V			1.5	V
V _{IH}	Input high Level voltage	R _L = 27Ω; V _{DD} = 16 V V _{DS} = 0.5 V	3.2			V
I _{ISS}	Supply current from input pin	V _{DS} = 0V; V _{IN} = 5V		150	300	μA
V _{INCL}	Input-Source reverse clamp voltage	I _{IN} = -1mA I _{IN} = 1mA	-1 8		-0.3 11	V V
I _{DSS}	Zero input voltage drain current (V _{IN} = 0V)	V _{DS} = 50V; V _{IN} = V _{IL} ; V _{DS} < 35V; V _{IN} = V _{IL}			250 100	μA μA

Table 5. Switching⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 16V; I _D = 1A V _{gen} = 7V; R _{gen} = 10Ω		1100	1600	ns
t _r	Rise time			550	900	ns
t _{d(off)}	Turn-off delay time			200	400	ns
t _f	Fall time			100	200	ns
t _{d(on)}	Turn-on delay time	V _{DD} = 16V; I _D = 1A V _{gen} = 7V; R _{gen} = 1000Ω		1.2	1.8	μs
t _r	Rise time			1	1.5	μs
t _{d(off)}	Turn-off delay time			1.6	2.3	μs
t _f	Fall time			1.2	1.8	μs
(di/dt) _{on}	Turn-on current slope	V _{DD} = 16V; I _D = 1A V _{in} = 7V; R _{gen} = 10Ω		1.5		A/μs
Q _i	Total input charge	V _{DD} = 12V; I _D = 1A; V _{IN} = 7V		13		nC

1. Parameters guaranteed by design / characterization.

Table 6. On⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R _{DS(on)}	Static Drain-Source on resistance	V _{IN} = 7V; I _D = 1 A; T _j < 125 °C		0.15	0.3	Ω

1. Pulsed: pulse duration = 300μs, duty cycle 1.5%.

Table 7. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{OSS}	Output capacitance	$V_{DS} = 13V; f = 1MHz; V_{IN} = 0V$		350	500	pF

Table 8. Source Drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 1 A; V_{IN} = V_{IL}$		0.8	1.6	V
$t_{rr}^{(2)}$	Reverse recovery time			125		ns
$Q_{rr}^{(2)}$	Reverse recovery charge	$I_{SD} = 1A; di/dt = 100 A/\mu s$ $V_{DD} = 30V; T_j = 25^\circ C$		0.22		μC
$I_{RRM}^{(2)}$	Reverse recovery current			3.5		A

1. Pulsed: pulse duration = 300 μ s, duty cycle 1.5%.

2. Parameters guaranteed by design / characterization.

Table 9. Protections (-40°C < T_j < 150°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{lim}	Drain current limit	$V_{IN} = 7V; V_{DS}=13V$	6	10	15	A
$t_{dlim}^{(1)}$	Step response current limit	$V_{IN} = 7 V; V_{DS}$ step from 0 to 13V		12	20	μs
$T_{jsh}^{(1)}$	Overttemperature shutdown		150			$^\circ C$
$T_{jrs}^{(1)}$	Overttemperature reset		135			$^\circ C$
$E_{as}^{(1)}$	Single pulse avalanche energy	Starting $T_j = 25^\circ C; V_{DD} = 24V$ $V_{IN} = 7V R_{gen} = 1k\Omega; L = 10mH$	250			mJ

1. Parameters guaranteed by design / characterization.

Figure 2. Switching waveforms