MOSFETs Silicon N-Channel MOS (DTMOSⅣ)

TK7A65W

1. Applications

- Switching Voltage Regulators

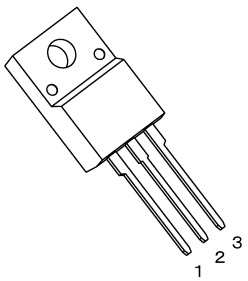
2. Features

(1) Low drain-source on-resistance: $R_{DS(ON)}$ = 0.64 Ω(typ.)
by using Super Junction Structure : DTMOS

(2) Easy to control Gate switching

(3) Enhancement mode: V_{th} = 2.5 to 3.5 V(V_{DS} = 10 V, I_D = 0.25 mA)

3. Packaging and Internal Circuit



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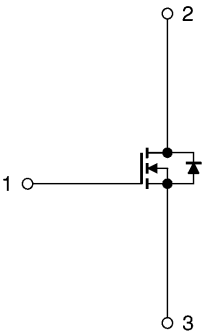


1: Gate
2: Drain
3: Source

4. Absolute Maximum Ratings (Note) (T_a = 25 °C unless otherwise specified)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	650	V
Gate-source voltage		V_{GSS}	±30	
Drain current (DC)	(Note 1)	I_D	6.8	A
Drain current (pulsed)	(Note 1)	I_{DP}	27.2	
Power dissipation	(T_c = 25 °C)	P_D	30	W
Single-pulse avalanche energy	(Note 2)	E_{AS}	90	mJ
Avalanche current		I_{AR}	1.7	A
Reverse drain current (DC)	(Note 1)	I_{DR}	6.8	
Reverse drain current (pulsed)	(Note 1)	I_{DRP}	27.2	
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	-55 to 150	
Isolation voltage (RMS)	(t = 1.0 s)	$V_{ISO(RMS)}$	2000	V
Mounting torque		TOR	0.6	N · m

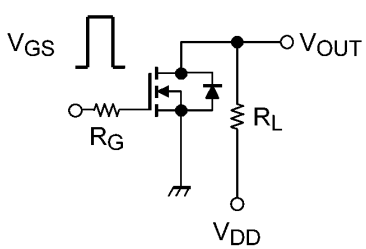
6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V	—	—	±1	μA
Drain cut-off current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	I_D = 10 mA, V_{GS} = 0 V	650	—	—	V
Gate threshold voltage	V_{th}	V_{DS} = 10 V, I_D = 0.25 mA	2.5	—	3.5	
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 3.4 A	—	0.64	0.78	Ω

6.2. Dynamic Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = 300 V, V_{GS} = 0 V, f = 1 MHz	—	490	—	pF
Reverse transfer capacitance	C_{rss}		—	1.7	—	
Output capacitance	C_{oss}		—	13	—	
Effective output capacitance	$C_{o(er)}$	V_{DS} = 0 to 400 V, V_{GS} = 0 V	—	21	—	
Gate resistance	r_g	V_{DS} = OPEN , f = 1 MHz	—	7	—	Ω
Switching time (rise time)	t_r	See Figure 6.2.1	—	13	—	ns
Switching time (turn-on time)	t_{on}		—	35	—	
Switching time (fall time)	t_f		—	4	—	
Switching time (turn-off time)	t_{off}		—	52	—	
MOSFET dv/dt ruggedness	dv/dt	V_{DD} = 0 to 400 V, I_D = 3.4 A	50	—	—	V/ns



V_{DD} ≈ 400 V
V_{GS} = 10 V/0 V
I_D = 3.4 A
R_L = 117 Ω
R_G = 10 Ω
Duty ≤ 1 %, t_w = 10 μs

Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD} ≈ 400 V, V_{GS} = 10 V, I_D = 6.8 A	—	15	—	nC
Gate-source charge 1	Q_{gs1}		—	3.2	—	
Gate-drain charge	Q_{gd}		—	7	—	

6.4. Source-Drain Characteristics (T_a = 25 °C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage	V_{DSF}	I_{DR} = 6.8 A, V_{GS} = 0 V	—	—	-1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 3.4 A, V_{GS} = 0 V $-dI_{DR}/dt$ = 100 A/μs	—	180	—	ns
Reverse recovery charge	Q_{rr}		—	1.7	—	μC
Peak reverse recovery current	I_{rr}		—	16	—	A
Diode dv/dt ruggedness	dv/dt	I_{DR} = 3.4 A, V_{GS} = 0 V, V_{DD} = 400 V	15	—	—	V/ns