MOSFETs Silicon N-channel MOS (U-MOSⅧ-H)

TK65A10N1

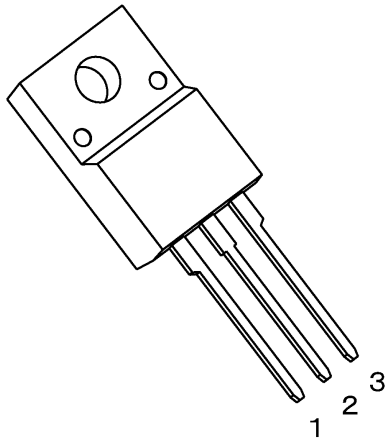
1. Applications

- Switching Voltage Regulators

2. Features

(1) Low drain-source on-resistance: $R_{DS(ON)}$ = 4.0 mΩ (typ.) (V_{GS} = 10 V)
(2) Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 100 V)
(3) Enhancement mode: V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_D = 1.0 mA)

3. Packaging and Internal Circuit



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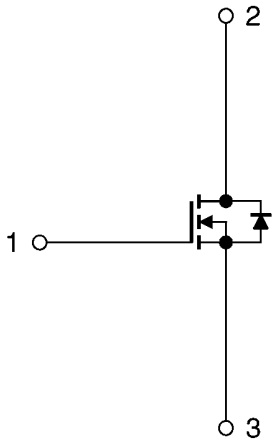


1: Gate
2: Drain
3: Source

4. Absolute Maximum Ratings (Note) (T_a = 25°C unless otherwise specified)

Characteristics			Symbol	Rating	Unit
Drain-source voltage			V_{DSS}	100	V
Gate-source voltage			V_{GSS}	±20	
Drain current (DC)	(Silicon limit)	(Note 1,2)	I_D	148	A
Drain current (DC)	(T_c = 25°C)	(Note 1)	I_D	65	
Drain current (pulsed)	(t = 1 ms)	(Note 1)	I_{DP}	296	
Power dissipation	(T_c = 25°C)		P_D	45	W
Single-pulse avalanche energy		(Note 3)	E_{AS}	143	mJ
Avalanche current			I_{AR}	65	A
Channel temperature			T_{ch}	150	°C
Storage temperature			T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

6. Electrical Characteristics

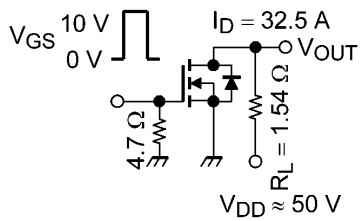
6.1. Static Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±0.1	μA
Drain cut-off current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	I_D = 10 mA, V_{GS} = 0 V	100	—	—	V
Drain-source breakdown voltage (Note 4)	$V_{(BR)DSX}$	I_D = 10 mA, V_{GS} = -20 V	65	—	—	
Gate threshold voltage	V_{th}	V_{DS} = 10 V, I_D = 1.0 mA	2.0	—	4.0	
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 32.5 A	—	4.0	4.8	mΩ

Note 4: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

6.2. Dynamic Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	—	5400	—	pF
Reverse transfer capacitance	C_{rss}		—	42	—	
Output capacitance	C_{oss}		—	950	—	
Gate resistance	r_g	—	—	2.4	—	Ω
Switching time (rise time)	t_r	See Figure 6.2.1	—	19	—	ns
Switching time (turn-on time)	t_{on}		—	44	—	
Switching time (fall time)	t_f		—	26	—	
Switching time (turn-off time)	t_{off}		—	85	—	



Duty ≤ 1%, t_w = 10 μs

Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD} ≈ 80 V, V_{GS} = 10 V, I_D = 65 A	—	81	—	nC
Gate-source charge 1	Q_{gs1}		—	31	—	
Gate-drain charge	Q_{gd}		—	18	—	
Gate switch charge	Q_{SW}		—	32	—	

8. Characteristics Curves (Note)

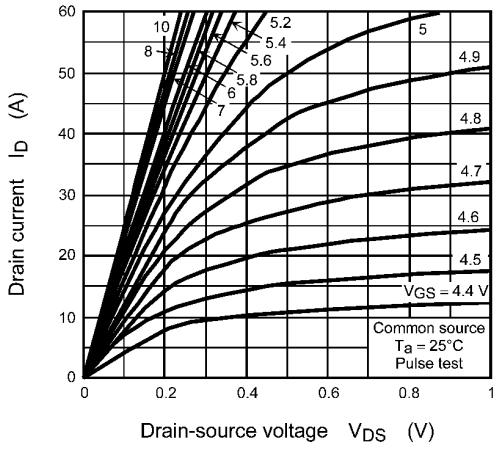


Fig. 8.1 I_D - V_{DS}

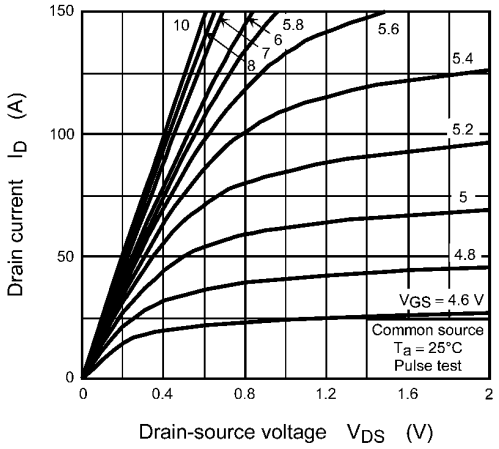


Fig. 8.2 I_D - V_{DS}

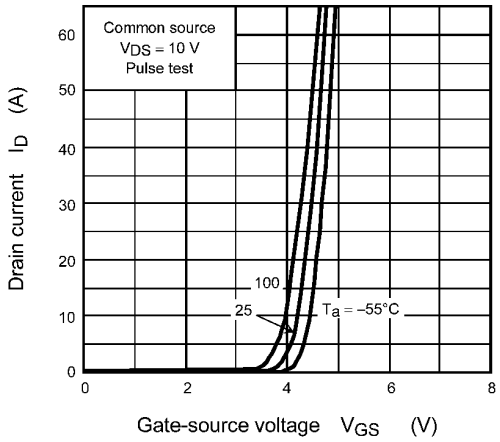


Fig. 8.3 I_D - V_{GS}

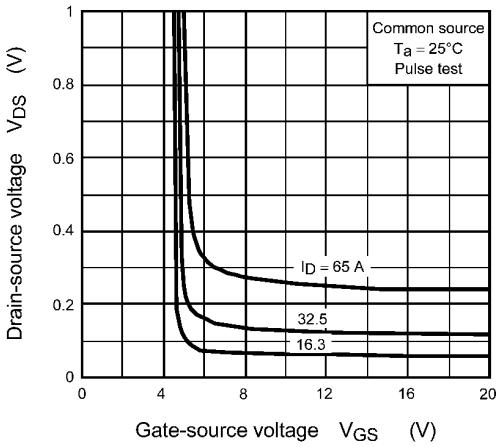


Fig. 8.4 V_{DS} - V_{GS}

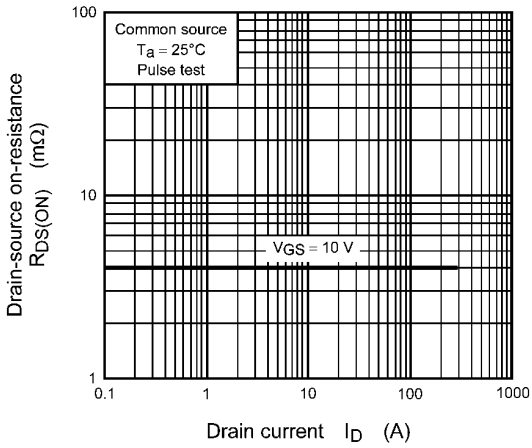


Fig. 8.5 $R_{DS(ON)}$ - I_D

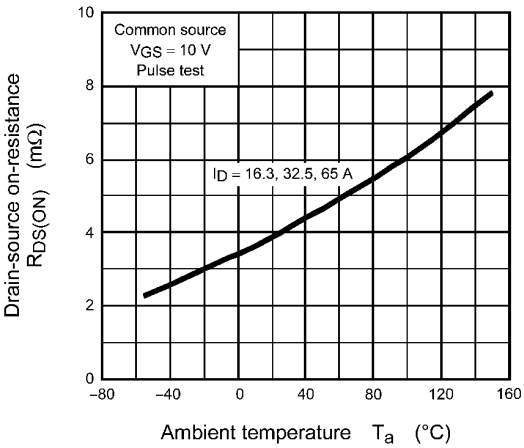


Fig. 8.6 $R_{DS(ON)}$ - T_a