

MOSFETs Silicon N-channel MOS (U-MOSVIII-H)

TK34A10N1



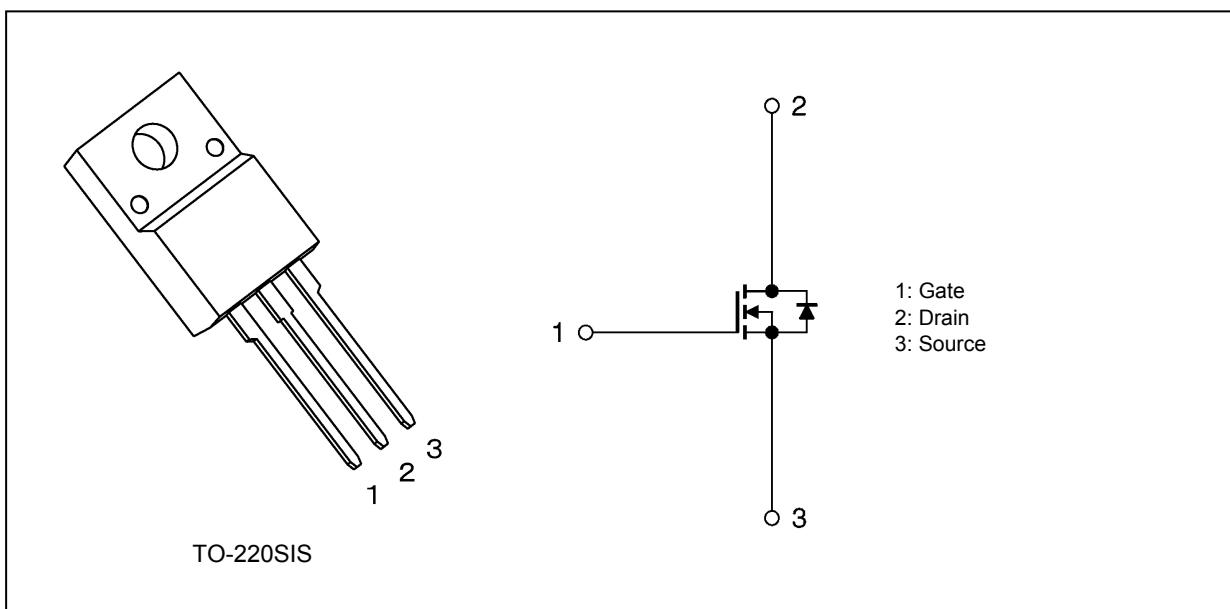
1. Applications

- Switching Voltage Regulators

2. Features

- (1) Low drain-source on-resistance: $R_{DS(ON)} = 7.9 \text{ m}\Omega$ (typ.) ($V_{GS} = 10 \text{ V}$)
- (2) Low leakage current: $I_{DSS} = 10 \mu\text{A}$ (max) ($V_{DS} = 100 \text{ V}$)
- (3) Enhancement mode: $V_{th} = 2.0$ to 4.0 V ($V_{DS} = 10 \text{ V}$, $I_D = 0.5 \text{ mA}$)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) ($T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics | Symbol | Rating | Unit |
|--|-----------|------------|------------------|
| Drain-source voltage | V_{DSS} | 100 | V |
| Gate-source voltage | V_{GSS} | ± 20 | |
| Drain current (DC) (Silicon limit) | I_D | 75 | A |
| Drain current (DC) ($T_c = 25^\circ\text{C}$) | I_D | 34 | |
| Drain current (pulsed) ($t = 1 \text{ ms}$) | I_{DP} | 147 | |
| Power dissipation ($T_c = 25^\circ\text{C}$) | P_D | 35 | W |
| Single-pulse avalanche energy | E_{AS} | 64 | mJ |
| Avalanche current | I_{AR} | 34 | A |
| Channel temperature | T_{ch} | 150 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -55 to 150 | |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

6. Electrical Characteristics

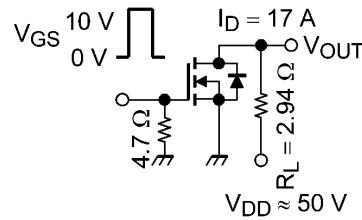
6.1. Static Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---------------|---|-----|------|-----------|------------------|
| Gate leakage current | I_{GSS} | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ | — | — | ± 0.1 | μA |
| Drain cut-off current | I_{DSS} | $V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$ | — | — | 10 | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$ | 100 | — | — | |
| Drain-source breakdown voltage (Note 4) | $V_{(BR)DSX}$ | $I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$ | 65 | — | — | |
| Gate threshold voltage | V_{th} | $V_{DS} = 10\text{ V}, I_D = 0.5\text{ mA}$ | 2.0 | — | 4.0 | |
| Drain-source on-resistance | $R_{DS(ON)}$ | $V_{GS} = 10\text{ V}, I_D = 17\text{ A}$ | — | 7.9 | 9.5 | $\text{m}\Omega$ |

Note 4: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

6.2. Dynamic Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|--------------------------------|-----------|---|-----|------|-----|-------------|
| Input capacitance | C_{iss} | $V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | — | 2600 | — | pF |
| Reverse transfer capacitance | C_{rss} | | — | 23 | — | |
| Output capacitance | C_{oss} | | — | 450 | — | |
| Gate resistance | r_g | — | — | 2.1 | — | Ω |
| Switching time (rise time) | t_r | See Figure 6.2.1 | — | 12 | — | ns |
| Switching time (turn-on time) | t_{on} | | — | 31 | — | |
| Switching time (fall time) | t_f | | — | 18 | — | |
| Switching time (turn-off time) | t_{off} | | — | 50 | — | |



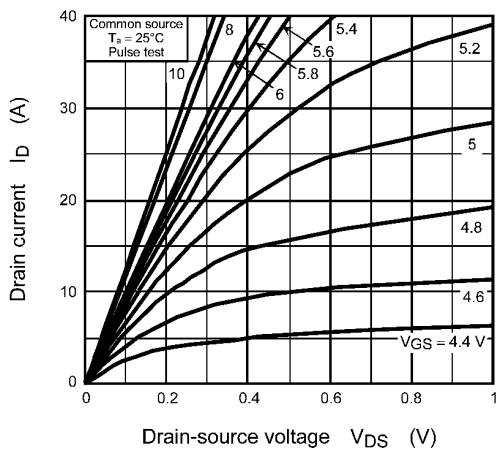
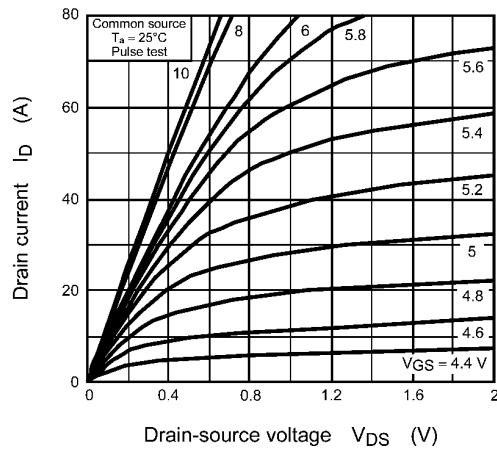
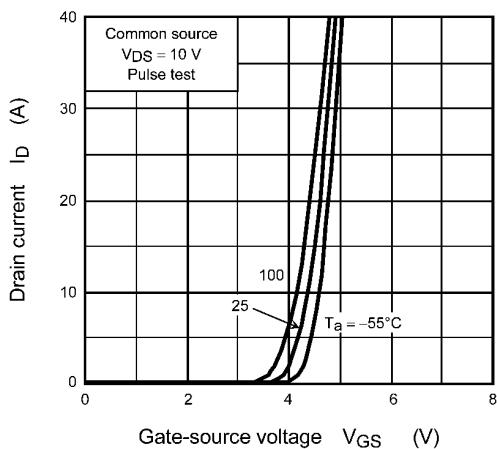
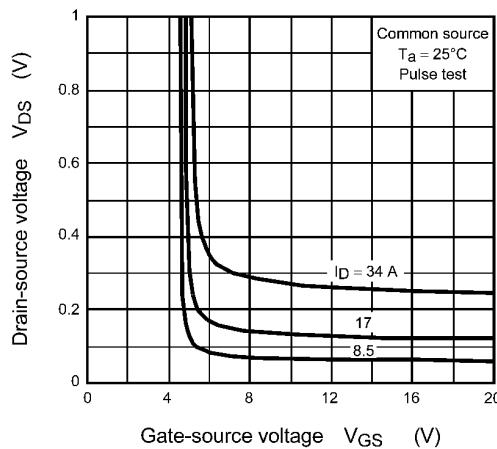
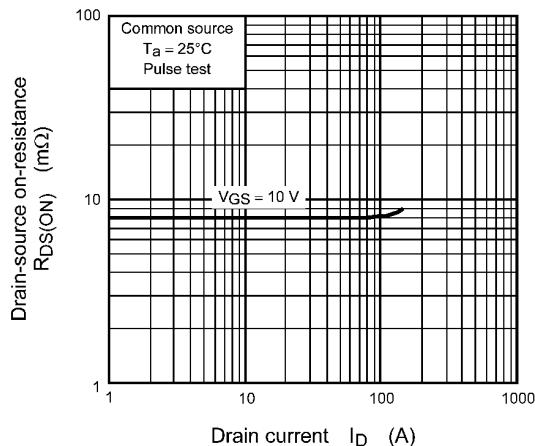
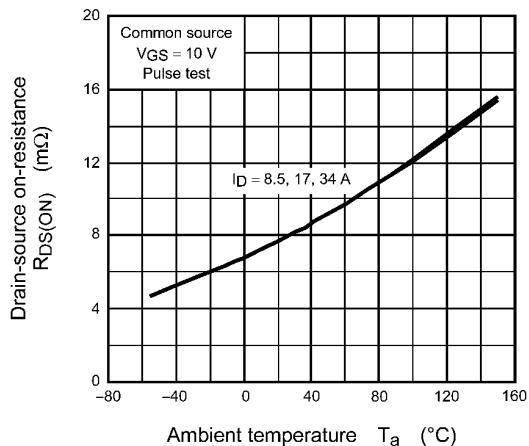
Duty $\leq 1\%$, $t_w = 10\text{ }\mu\text{s}$

Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|-----------|---|-----|------|-----|-------------|
| Total gate charge (gate-source plus gate-drain) | Q_g | $V_{DD} \approx 80\text{ V}, V_{GS} = 10\text{ V}, I_D = 34\text{ A}$ | — | 38 | — | nC |
| Gate-source charge 1 | Q_{gs1} | | — | 13 | — | |
| Gate-drain charge | Q_{gd} | | — | 9.7 | — | |
| Gate switch charge | Q_{sw} | | — | 15 | — | |

8. Characteristics Curves (Note)

Fig. 8.1 I_D - V_{DS}Fig. 8.2 I_D - V_{DS}Fig. 8.3 I_D - V_{GS}Fig. 8.4 V_{DS} - V_{GS}Fig. 8.5 R_{DS(ON)} - I_DFig. 8.6 R_{DS(ON)} - T_a