MOSFETs Silicon N-Channel MOS (π-MOSⅦ)

TK18A30D

1. Applications

- Switching Voltage Regulators

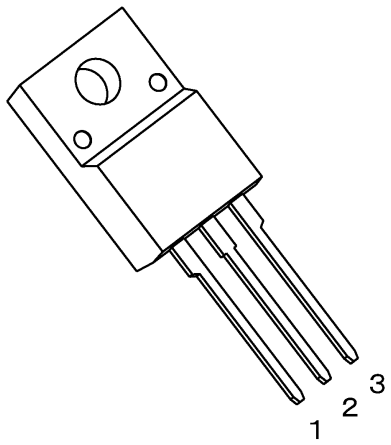
2. Features

(1) Low drain-source on-resistance: $R_{DS(ON)}$ = 0.1 Ω (typ.)

(2) Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 300 V)

(3) Enhancement mode: V_{th} = 1.5 to 3.5 V (V_{DS} = 10 V, I_D = 1 mA)

3. Packaging and Internal Circuit



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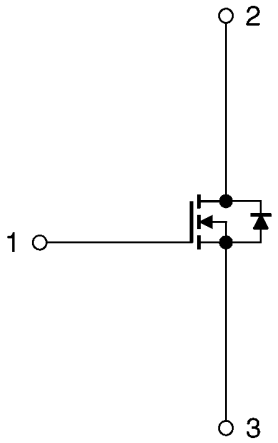


1: Gate (G)
2: Drain (D)
3: Source (S)

4. Absolute Maximum Ratings (Note) (T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	300	V
Gate-source voltage		V_{GSS}	±20	
Drain current (DC)	(Note 1)	I_D	18	A
Drain current (pulsed)	(Note 1)	I_{DP}	72	
Power dissipation	(T_c = 25°C)	P_D	45	W
Single-pulse avalanche energy	(Note 2)	E_{AS}	126	mJ
Avalanche current	(Note 3)	I_{AR}	18	A
Reverse drain current (DC)	(Note 1)	I_{DR}	18	
Reverse drain current (pulsed)	(Note 1)	I_{DRP}	72	
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	-55 to 150	
Isolation voltage (RMS)	(t = 1.0 s)	$V_{ISO(RMS)}$	2000	V
Mounting torque		TOR	0.6	N · m

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	2.78	°C/W
Channel-to-ambient thermal resistance	$R_{th(ch-a)}$	62.5	

Note 1: Ensure that the channel temperature does not exceed 150°C.
Note 2: V_{DD} = 50 V, T_{ch} = 25°C (initial), L = 0.67 mH, R_G = 25 Ω, I_{AR} = 18 A
Note 3: Repetitive rating; pulse width limited by maximum channel temperature

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

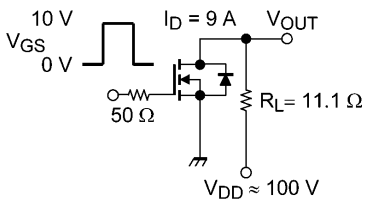
6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±1	μA
Drain cut-off current	I_{DSS}	V_{DS} = 300 V, V_{GS} = 0 V	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	I_D = 10 mA, V_{GS} = 0 V	300	—	—	V
Gate threshold voltage	V_{th}	V_{DS} = 10 V, I_D = 1 mA	1.5	—	3.5	
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 9 A	—	0.1	0.139	Ω

6.2. Dynamic Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	—	2600	—	pF
Reverse transfer capacitance	C_{rss}		—	17	—	
Output capacitance	C_{oss}		—	140	—	
Gate resistance	r_g	V_{DS} = OPEN, f = 1 MHz	—	6.3	—	Ω
Switching time (rise time)	t_r	See Figure 6.2.1.	—	70	—	ns
Switching time (turn-on time)	t_{on}		—	115	—	
Switching time (fall time)	t_f		—	55	—	
Switching time (turn-off time)	t_{off}		—	345	—	



Duty ≤ 1%, t_w = 10 μs

Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD} ≈ 240 V, V_{GS} = 10 V, I_D = 18 A	—	60	—	nC
Gate-source charge 1	Q_{gs1}		—	10	—	
Gate-drain charge	Q_{gd}		—	20	—	

6.4. Source-Drain Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage	V_{DSF}	I_{DR} = 18 A, V_{GS} = 0 V	—	—	-1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 18 A, V_{GS} = 0 V $-dI_{DR}/dt$ = 100 A/μs	—	250	—	ns
Reverse recovery charge	Q_{rr}		—	2.1	—	μC
Peak reverse recovery current	I_{rr}		—	16.5	—	A

8. Characteristics Curves (Note)

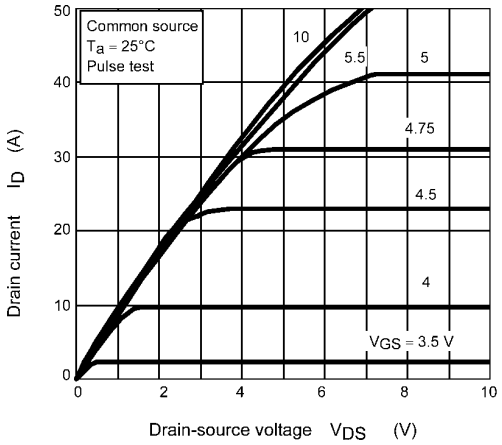


Fig. 8.1 I_D - V_{DS}

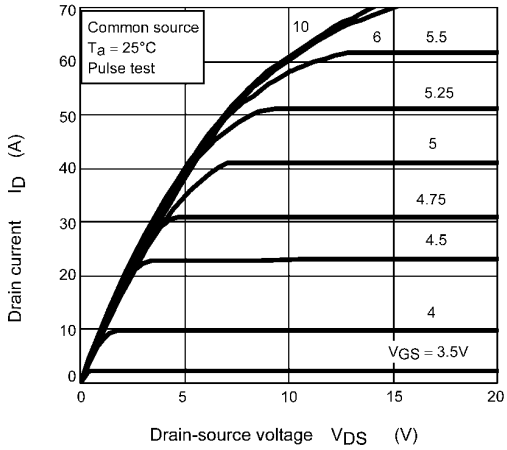


Fig. 8.2 I_D - V_{DS}

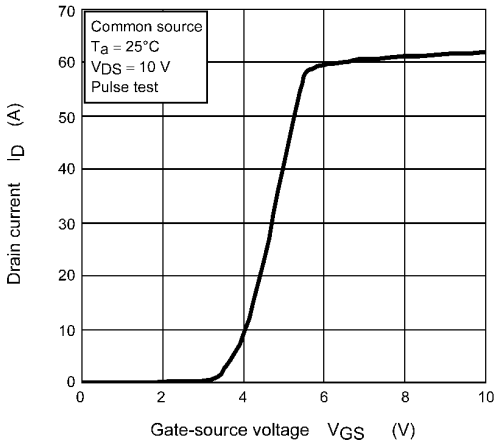


Fig. 8.3 I_D - V_{GS}

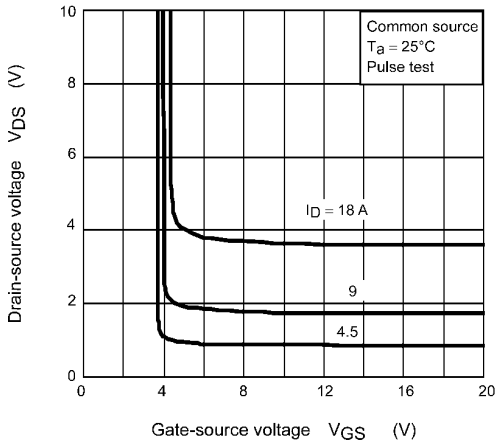


Fig. 8.4 V_{DS} - V_{GS}

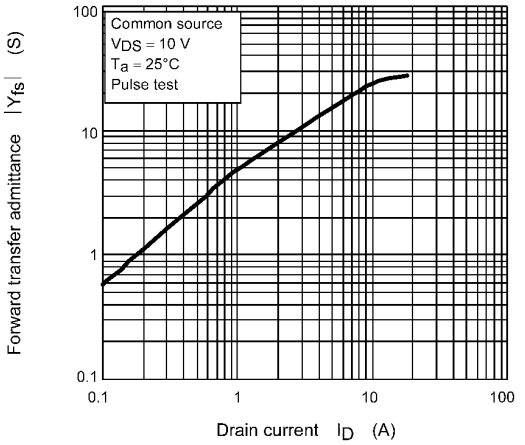


Fig. 8.5 $|Y_{fs}|$ - I_D

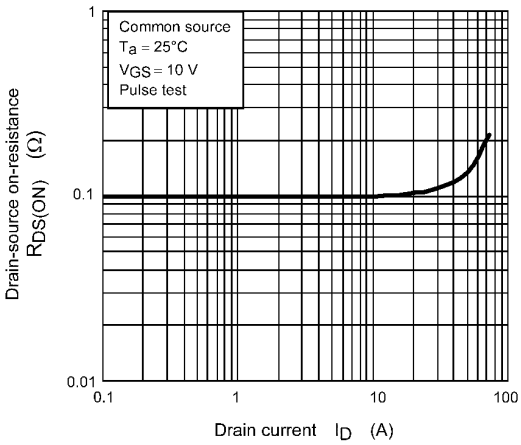


Fig. 8.6 $R_{DS(ON)}$ - I_D