STB12NM60N/-1 - STF12NM60N STP12NM60N - STW12NM60N

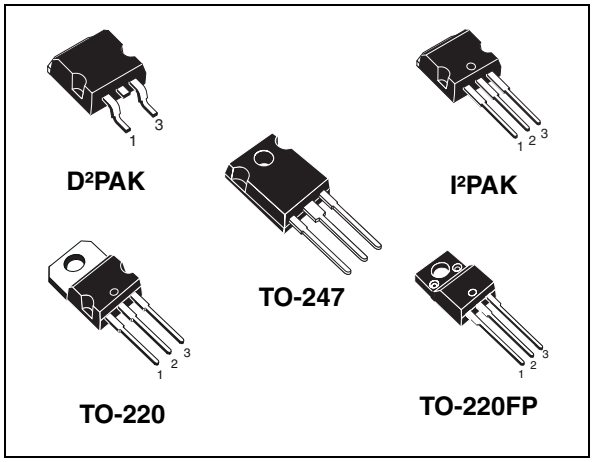
N-channel 600V - 0.35Ω - 10A - D^2/I^2PAK - TO-220/FP - TO-247
Second generation MDmesh™ Power MOSFET

Features

Type	V_{DSS} (@Tjmax)	$R_{DS(on)}$	I_D
STB12NM60N	650V	< 0.41Ω	10A
STB12NM60N-1	650V	< 0.41Ω	10A
STF12NM60N	650V	< 0.41Ω	10A(1)
STP12NM60N	650V	< 0.41Ω	10A
STW12NM60N	650V	< 0.41Ω	10A

1. Limited only by maximum temperature allowed

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



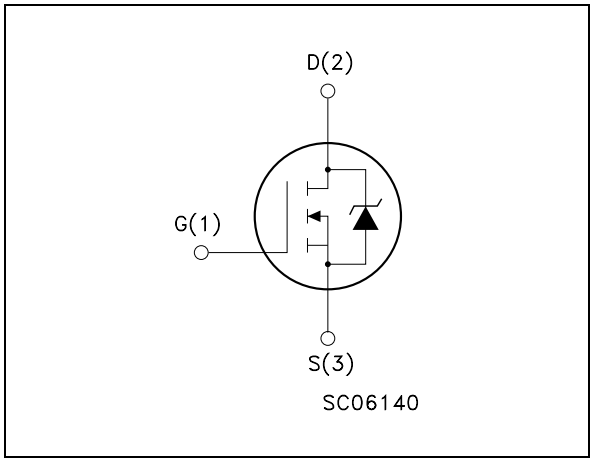
Description

This series of devices implements second generation MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the Company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Application

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB12NM60N	B12NM60N	D²PAK	Tape & reel
STB12NM60N-1	B12NM60N	I²PAK	Tube
STF12NM60N	F12NM60N	TO-220FP	Tube
STP12NM60N	P12NM60N	TO-220	Tube
STW12NM60N	W12NM60N	TO-247	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D²PAK/I²PAK TO-220/TO-247	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS}=0)	600		V
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at T_C = 25°C	10	10 (1)	A
I_D	Drain current (continuous) at T_C = 100°C	6.3	6.3 (1)	A
I_{DM} (2)	Drain current (pulsed)	40	40 (1)	A
P_{TOT}	Total dissipation at T_C = 25°C	90	25	W
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s;T_C=25°C)	--	2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤10A, di/dt ≤400A/µs, V_{DD} =80% $V_{(BR)DSS}$

Table 2. Thermal data

Symbol	Parameter	D²PAK/I²PAK TO-220/TO-247	TO-220FP	Unit
Rthj-case	Thermal resistance junction-case max	1.38	5	°C/W
Rthj-amb	Thermal resistance junction-amb max	62.5		°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max)	3.5	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, I_D=I_{AS}, V_{DD}= 50V)	200	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS}= 0	600			V
dv/dt(1)	Drain-source voltage slope	V_{DD} = 400V,I_D = 10A, V_{GS} = 10V		41		V/ns
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating, @125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 5A		0.35	0.41	Ω

1. Characteristics value at turn off on inductive load

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}(1)	Forward transconductance	V_{DS} =15V, I_D= 5A		8		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50V, f =1MHz, V_{GS} = 0		960 65 7		pF pF pF
$C_{oss\ eq.}$(2)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0V to 480V		180		pF
Rg	Gate input resistance	f=1MHz Gate DC Bias=0 Test signal level=20mV open drain		5		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 480V, I_D = 10A V_{GS} = 10V		30.5 5 16		nC nC nC

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 300V, I_D = 5A, R_G = 4.7Ω, V_{GS} = 10V		15 9 60 10		ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				10 40	A A
V_{SD}(2)	Forward on voltage	I_{SD} = 10A, V_{GS}=0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} =10A, di/dt =100A/µs, V_{DD} = 100V, Tj = 25°C		360 3.5 20		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	V_{DD} = 100V di/dt =100A/µs, I_{SD} = 10A Tj = 150°C		530 5.20 20		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220 / D²PAK / I²PAK

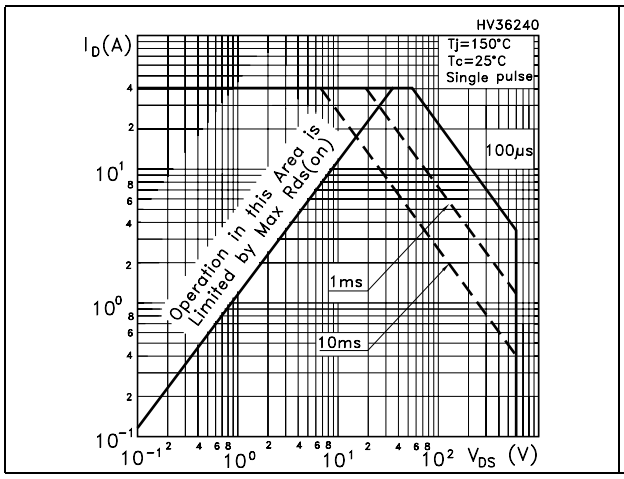


Figure 2. Thermal impedance for TO-220 / D²PAK / I²PAK

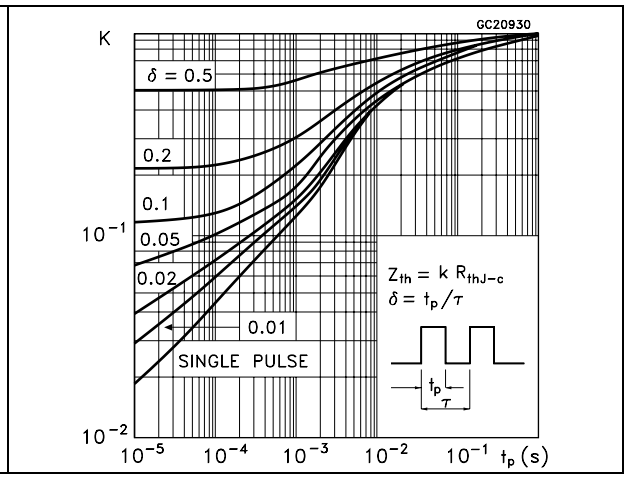


Figure 3. Safe operating area for TO-220FP

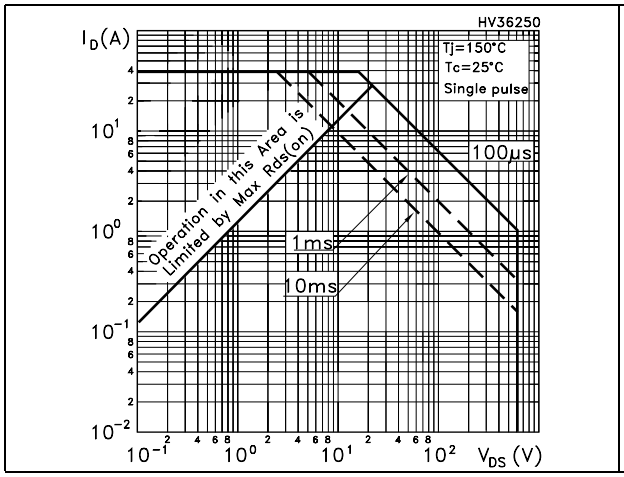


Figure 4. Thermal impedance for TO-220FP

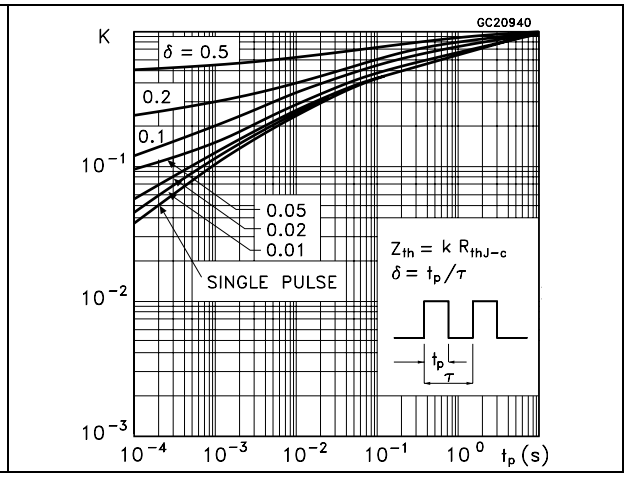


Figure 5. Safe operating area for TO-247

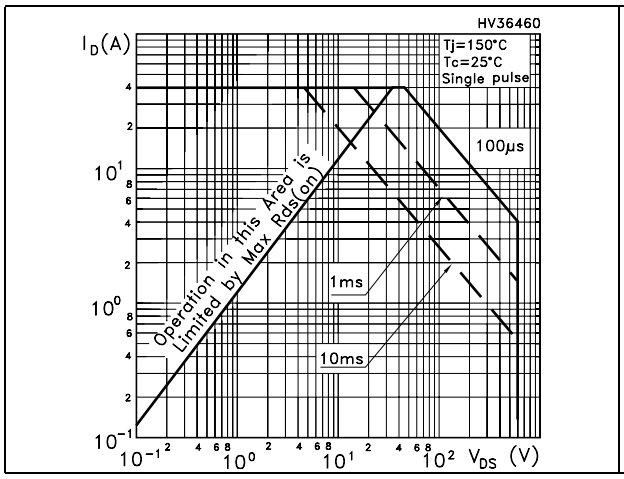


Figure 6. Thermal impedance for TO-247