

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STY80NM60N	600 V	< 0.040 Ω	80 A	560 W

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Application

- Switching applications

## Description

This series of devices implements second generation MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the Company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

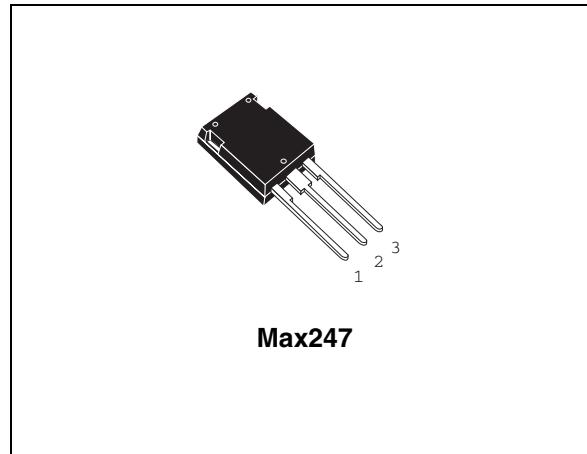


Figure 1. Internal schematic diagram

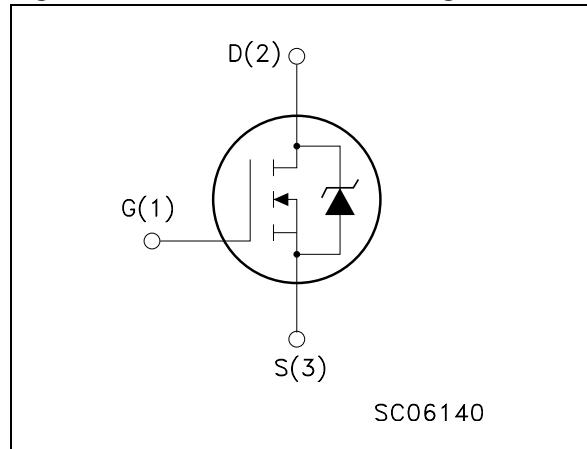


Table 1. Device summary

Order code	Marking	Package	Packaging
STY80NM60N	80NM60N	Max247	Tube

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	600	V
$V_{GS}$	Gate- source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	80	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	50.4	A
$I_{DM}^{(1)}$	Drain current (pulsed)	320	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	560	W
	Derating factor	4.48	W/ $^\circ\text{C}$
$dV/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area  
 2.  $I_{SD} \leq 80\text{A}$ ,  $di/dt \leq 400 \text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\%$   $V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.22	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	30	$^\circ\text{C}/\text{W}$
$T_I$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ Max)	Tbd	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25^\circ\text{C}$ , $I_d=I_{AS}$ , $V_{dd}=50\text{ V}$ )	Tbd	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	600			V
$dv/dt^{(1)}$	Drain source voltage slope	$V_{DD} = 480 \text{ V}, I_D = 80 \text{ A}, V_{GS} = 10 \text{ V}$		Tbd		V/ns
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating, @ } 125^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 \text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 40 \text{ A}$		0.035	0.04	$\Omega$

1. Characteristic value at turn off on inductive load

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS}=15 \text{ V}, I_D=40 \text{ A}$		Tbd		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50 \text{ V}, f = 1 \text{ MHz}$ , $V_{GS} = 0$		Tbd Tbd Tbd		pF pF pF
$C_{oss eq.}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0 \text{ V}, V_{DS} = 0 \text{ V to } 480 \text{ V}$		Tbd		pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 480 \text{ V}, I_D = 80 \text{ A},$ $V_{GS} = 10 \text{ V}$ ,		Tbd Tbd Tbd		nC nC nC
$R_g$	Gate input resistance	f=1MHz Gate DC Bias=0 Test signal level = 20 mV open drain		Tbd		$\Omega$

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

2.  $C_{oss eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time			Tbd		ns
$t_r$	Rise time			Tbd		ns
$t_{d(off)}$	Turn-off delay time			Tbd		ns
$t_f$	Fall time			Tbd		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				320	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 80 \text{ A}, V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 80 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		Tbd		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100 \text{ V}, T_j = 25 \text{ }^\circ\text{C}$		Tbd		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			Tbd		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 80 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		Tbd		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$		Tbd		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			Tbd		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%