

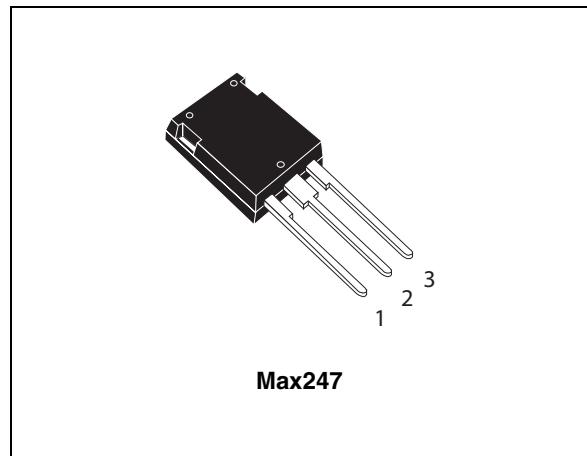
N-channel 650 V, 0.014 Ω typ., 130 A, MDmesh™ V Power MOSFET in Max247 package

Datasheet — production data

Features

Order code	V_{DS} @ T_{jMAX}	$R_{DS(on)}$ max	I_D
STY139N65M5	710 V	0.017 Ω	130 A

- Max247 worldwide best $R_{DS(on)}$
- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested



Applications

- Switching applications

Description

The device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESHTM horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram

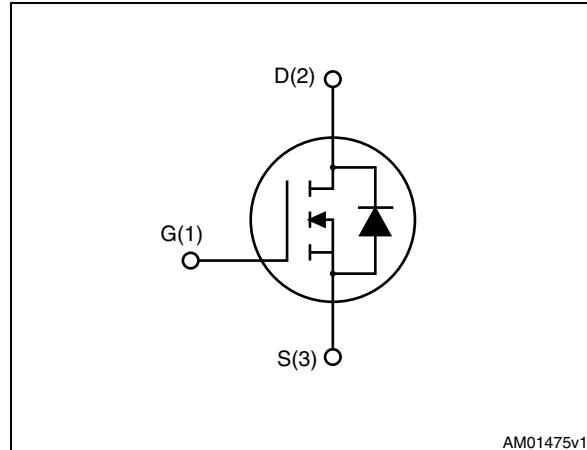


Table 1. Device summary

Order code	Marking	Package	Packaging
STY139N65M5	139N65M5	Max247	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	130	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	78	A
$I_{DM}^{(1)}$	Drain current (pulsed)	520	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	625	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	17	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{V}$)	2400	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 130 \text{ A}$, $di/dt = 400 \text{ A}/\mu\text{s}$, $V_{DD} = 400 \text{ V}$, peak $V_{DS} < V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.2	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	30	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

2 Electrical characteristics

($T_C = 25^\circ\text{C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650 \text{ V}$ $V_{DS} = 650 \text{ V}, T_C = 125^\circ\text{C}$			10 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25 \text{ V}$			± 100	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 65 \text{ A}$		0.014	0.017	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz},$ $V_{GS} = 0$	-	15600 365 9	-	pF pF pF
$C_{o(\text{tr})}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0 \text{ to } 520 \text{ V}$	-	1559	-	pF
$C_{o(\text{er})}^{(2)}$	Equivalent capacitance energy related	$V_{GS} = 0, V_{DS} = 0 \text{ to } 520 \text{ V}$	-	360	-	pF
R_G	Intrinsic gate resistance	$f = 1 \text{ MHz open drain}$	-	1.2	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 520 \text{ V}, I_D = 65 \text{ A},$ $V_{GS} = 10 \text{ V}$	-	363 88 164	-	nC nC nC

1. $C_{o(\text{tr})}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
2. $C_{o(\text{er})}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400 \text{ V}$, $I_D = 80 \text{ A}$,		295		ns
$t_{r(v)}$	Voltage rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$	-	56	-	ns
$t_{f(i)}$	Current fall time			37		ns
$t_{c(off)}$	Crossing time			84		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current			130		A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	520		A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 130 \text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 130 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$		570		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100 \text{ V}$ (see)	-	15		μC
I_{RRM}	Reverse recovery current			53		A
t_{rr}	Reverse recovery time	$I_{SD} = 130 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$		720		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100 \text{ V}$, $T_j = 150^\circ\text{C}$	-	24		μC
I_{RRM}	Reverse recovery current			68		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

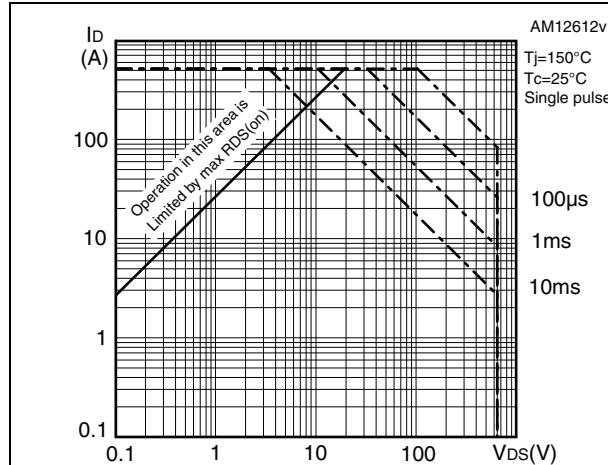


Figure 3. Thermal impedance

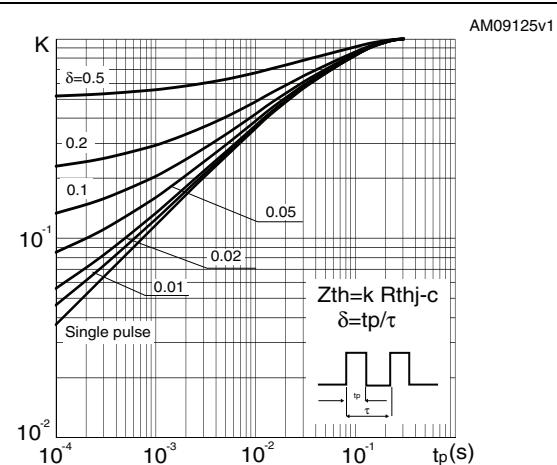


Figure 4. Output characteristics

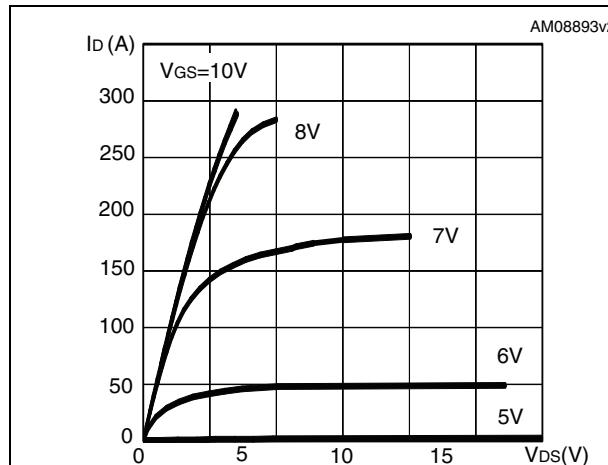


Figure 5. Transfer characteristics

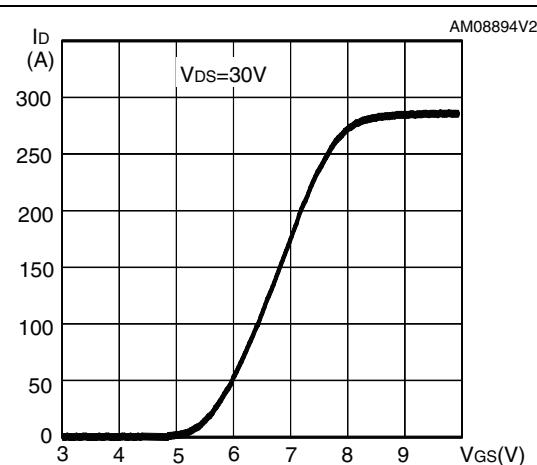


Figure 6. Normalized B_{VDSS} vs temperature

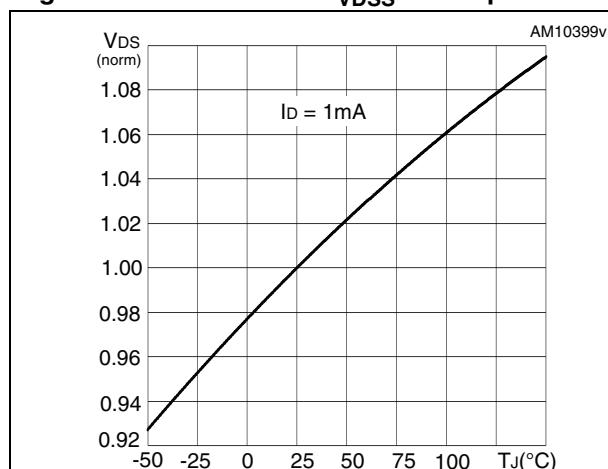


Figure 7. Static drain-source on resistance

