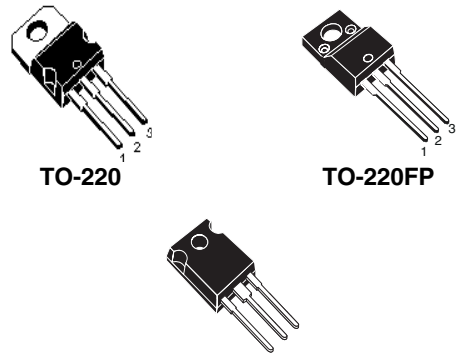
STP8NK80Z - STP8NK80ZFP
STW8NK80Z

N-channel 800V - 1.3Ω - 6.2A - TO-220 /TO-220FP/TO-247
Zener-protected SuperMESH™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STP8NK80Z	800 V	< 1.5 Ω	6.2 A
STP8NK80ZFP	800 V	< 1.5 Ω	6.2 A
STW8NK80Z	800 V	< 1.5 Ω	6.2 A

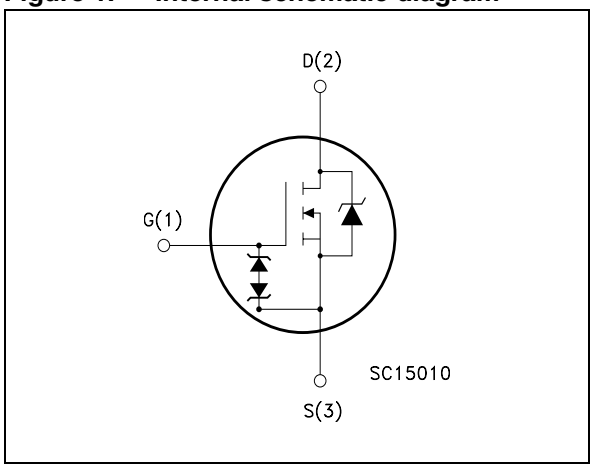
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Figure 1. Internal schematic diagram



Application

- Switching applications

Table 1. Device summary

Order codes	Marking	Package	Packaging
STP8NK80Z	P8NK80Z	TO-220	Tube
STP8NK80ZFP	P8NK80ZFP	TO-220FP	Tube
STW8NK80Z	W8NK80Z	TO-247	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220 - TO-247	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	800		V
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25°C	6.2	6.2 (1)	A
I_D	Drain current (continuous) at T_C = 100°C	3.9	3.9 (1)	A
I_{DM} (2)	Drain current (pulsed)	24.8	24.8(1)	A
P_{TOT}	Total dissipation at T_C = 25°C	140	30	W
	Derating factor	1.12	0.24	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	4000		V
dv/dt (3)	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s; Tc= 25°C)	-	2500	V
T_j T_{stg}	Max operating Junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤6.2 A, di/dt ≤200A/µs, V_{DD} ≤$V_{(BR)DSS}$, T_j ≤T_{JMAX}.

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220	TO-220FP	TO-247	
$R_{thj-case}$	Thermal resistance junction-case max	0.89	4.2	0.89	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5		50	°C/W
T_l	Maximum lead temperature for soldering purpose	300			°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	6.2	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	300	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D =1mA, V_{GS} = 0	800			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, @125°C			1 50	µA µA
I_{GSS}	Gate-body leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 3.1 A		1.3	1.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15v, I_D = 3.1 A		5.2		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		1320 143 27		pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{DS} =0V, V_{DS} = 0V to 640V		58		pF
$t_{d(on)}$ t_r $t_{r(off)}$ t_r	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 400 V, I_D = 3.1 A, R_G = 4.7 Ω, V_{GS} = 10 V		17 30 48 28		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 640 V, I_D = 6.2 A, V_{GS} = 10 V		46 8.5 25		nC nC nC
$t_{r(Voff)}$ t_r t_c	Off-voltage rise time Fall time Cross-over time	V_{DD} = 640 V, I_D = 6.2 A, R_G = 4.7 Ω, V_{GS} = 10 V		9 9 18		ns ns ns

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)				6.2 24.8	A A
V_{SD}(2)	Forward on voltage	I_{SD} = 6.2 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 6.2 A, di/dt = 100 A/µs V_{DD} = 50 V, Tj = 150°C		460 2990 13		ns nC A

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. Pulse width limited by safe operating area

Table 8. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}(1)	Gate-source breakdown voltage	Igs=± 1mA (Open Drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

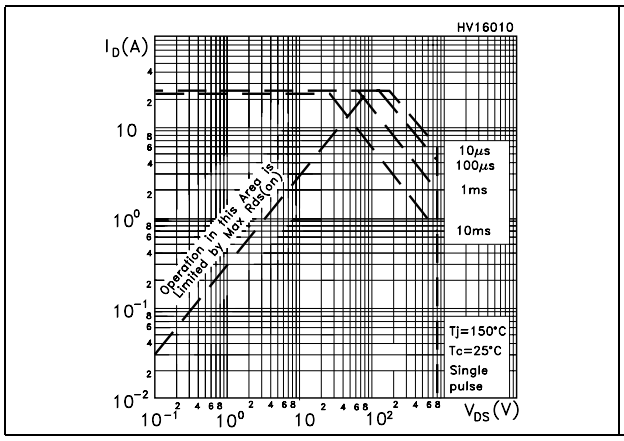


Figure 3. Thermal impedance for TO-220

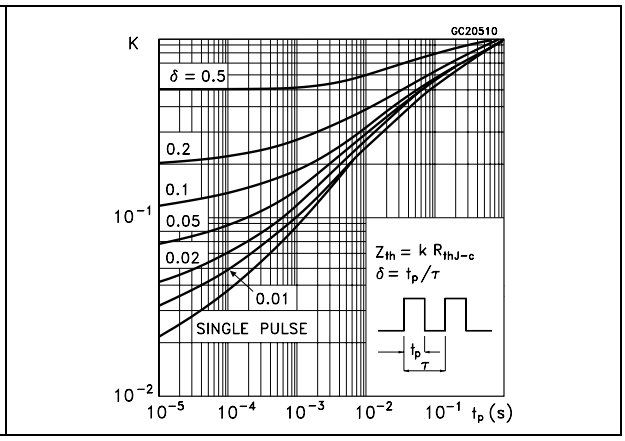


Figure 4. Safe operating area for TO-220FP

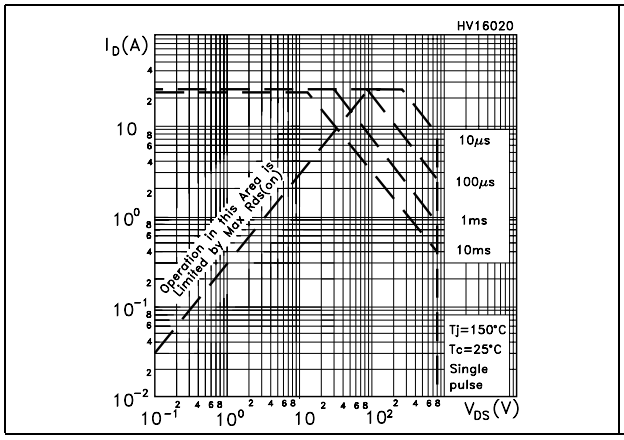


Figure 5. Thermal impedance for TO-220FP

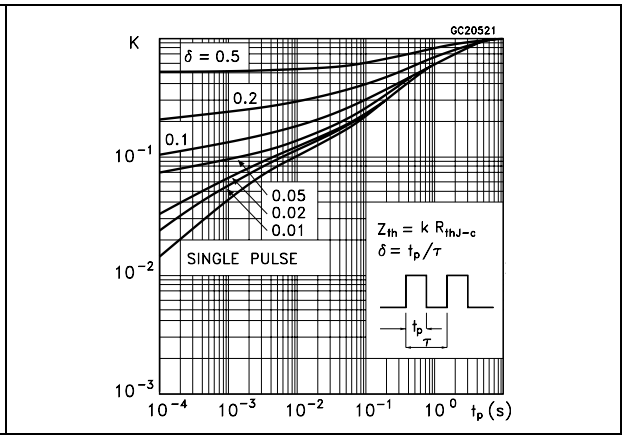


Figure 6. Safe operating area for TO-247

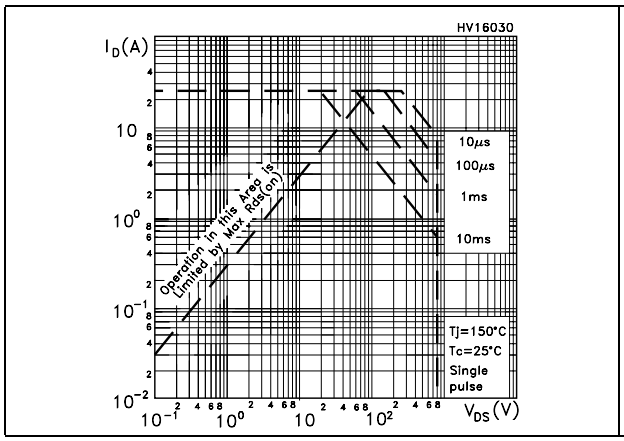


Figure 7. Thermal impedance for TO-247