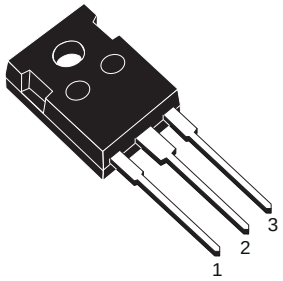
STW80NF10

N-CHANNEL 100V - 0.012Ω - 80A TO-247
LOW GATE CHARGE STripFET™ POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STW80NF10	100 V	< 0.015 Ω	80 A

- TYPICAL R_{DS}(on) = 0.012Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION

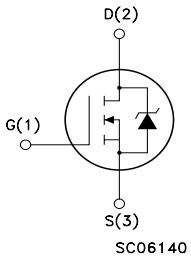


TO-247

DESCRIPTION

This Power Mosfet series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	100	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	100	V
V_{GS}	Gate- source Voltage	±20	V
I_D (*)	Drain Current (continuos) at T_C = 25°C	80	A
I_D	Drain Current (continuos) at T_C = 100°C	50	A
I_{DM} (●)	Drain Current (pulsed)	320	A
P_{TOT}	Total Dissipation at T_C = 25°C	300	W
	Derating Factor	2	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	9	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	245	mJ
T_{stg}	Storage Temperature	–65 to 175	°C
T_j	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area
(*) Limited by wire bonding

(1) I_{SD} ≤80A, di/dt ≤300A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ $T_{JMAX.}$
(2) Starting T_j = 25°C, I_D = 80A, V_{DD} = 50V

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	100			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 40 A		0.012	0.015	Ω
$I_{D(on)}$	On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, V_{GS} = 10V	80			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D =40 A		20		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		4300		pF
C_{oss}	Output Capacitance			600		pF
C_{rss}	Reverse Transfer Capacitance			240		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 50V, I_D = 40A R_G = 4.7Ω V_{GS} = 10V (see test circuit, Figure 3)		40		ns
t_r	Rise Time			145		ns
Q_g	Total Gate Charge	V_{DD} = 80V, I_D = 80A, V_{GS} = 10V		140	189	nC
Q_{gs}	Gate-Source Charge			23		nC
Q_{gd}	Gate-Drain Charge			51		nC

SWITCHING OFF

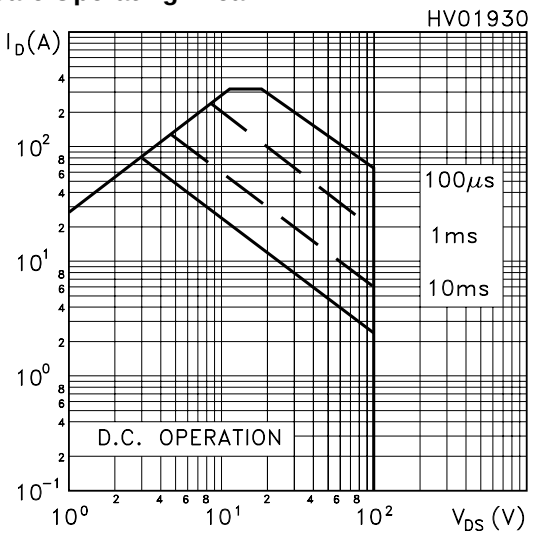
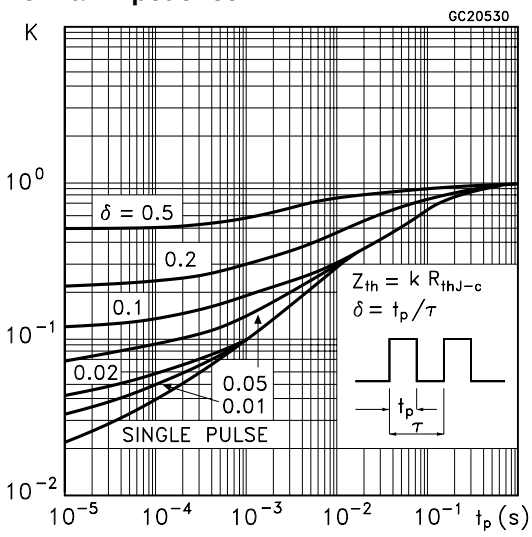
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	V_{DD} = 27V, I_D = 40A, R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 3)		134		ns
t_f	Fall Time			115		ns
$t_{d(off)}$	Off-voltage Rise Time	Vclamp =80V, I_D =80A R_G = 4.7Ω, V_{GS} = 10V		111		ns
t_f	Fall Time	(see test circuit, Figure 5)		125		ns
t_c	Cross-over Time			185		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				80	A
I_{SDM} (1)	Source-drain Current (pulsed)				320	A
V_{SD} (2)	Forward On Voltage	I_{SD} = 80A, V_{GS} = 0			1.5	V
t_{rr}	Reverse Recovery Time	I_{SD} = 80A, di/dt = 100A/µs, V_{DD} = 50V, T_j = 150°C (see test circuit, Figure 5)		155		ns
Q_{rr}	Reverse Recovery Charge			850		nC
I_{RRM}	Reverse Recovery Current			11		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Safe Operating Area



Thermal Impedence