

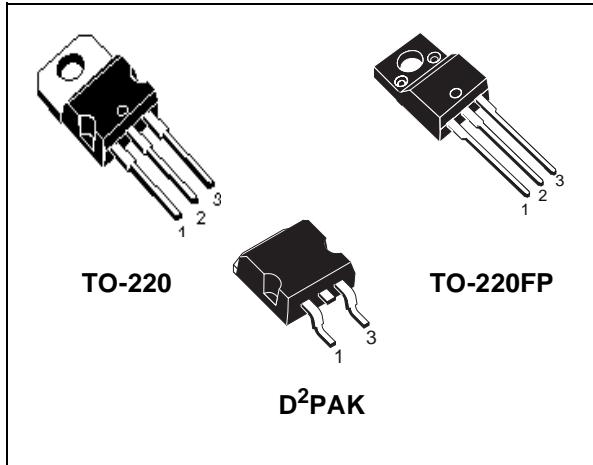


# STP6NK90Z - STP6NK90ZFP STB6NK90Z

N-CHANNEL 900V - 1.56Ω - 5.8A TO-220/TO-220FP/D<sup>2</sup>PAK  
Zener-Protected SuperMESH™ Power MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STP6NK90Z	900 V	< 2 Ω	5.8 A	140 W
STP6NK90ZFP	900 V	< 2 Ω	5.8 A	30 W
STB6NK90Z	900 V	< 2 Ω	5.8 A	140 W

- TYPICAL R<sub>DS(on)</sub> = 1.56 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY



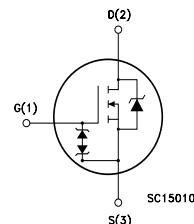
## DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

## APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING

## INTERNAL SCHEMATIC DIAGRAM



## ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP6NK90Z	P6NK90Z	TO-220	TUBE
STP6NK90ZFP	P6NK90ZFP	TO-220FP	TUBE
STB6NK90ZT4	B6NK90Z	D <sup>2</sup> PAK	TAPE & REEL

## STP6NK90Z - STP6NK90ZFP - STB6NK90Z

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP6NK90Z / STB6NK90Z	STP6NK90ZFP	
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	900		V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	900		V
$V_{GS}$	Gate- source Voltage	$\pm 30$		V
$I_D$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	5.8	5.8 (*)	A
$I_D$	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	3.65	3.65 (*)	A
$I_{DM} (\bullet)$	Drain Current (pulsed)	23.2	23.2 (*)	A
$P_{TOT}$	Total Dissipation at $T_C = 25^\circ\text{C}$	140	30	W
	Derating Factor	1.12	0.24	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5K $\Omega$ )	4000		V
$dv/dt$ (1)	Peak Diode Recovery voltage slope	4.5		V/ns
$V_{iso}$	Insulation Withstand Voltage (DC)	--	2500	V
$T_j$ $T_{stg}$	Operating Junction Temperature Storage Temperature	-55 to 150		$^\circ\text{C}$

(•) Pulse width limited by safe operating area

(1)  $I_{SD} \leq 5.8\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$ .

(\*) Limited only by maximum temperature allowed

### THERMAL DATA

		TO-220	D <sup>2</sup> PAK	TO-220FP	Unit
$R_{thj-case}$	Thermal Resistance Junction-case Max	0.89		4.2	$^\circ\text{C/W}$
$R_{thj-pcb}$	Thermal Resistance Junction-pcb Max (When mounted on minimum Footprint)		60		$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	62.5			$^\circ\text{C/W}$
$T_I$	Maximum Lead Temperature For Soldering Purpose	300			$^\circ\text{C}$

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
$I_{AR}$	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max)	5.8	A
$E_{AS}$	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	300	mJ

### GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1\text{mA}$ (Open Drain)	30			V

### PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## STP6NK90Z - STP6NK90ZFP - STB6NK90Z

### ELECTRICAL CHARACTERISTICS ( $T_{CASE} = 25^\circ\text{C}$ UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1\text{mA}$ , $V_{GS} = 0$	900			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ , $T_C = 125^\circ\text{C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 100\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$ , $I_D = 2.9\text{ A}$		1.56	2	$\Omega$

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_f(1)$	Forward Transconductance	$V_{DS} = 15\text{V}$ , $I_D = 2.9\text{ A}$		5		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		1350 130 26		pF pF pF
$C_{oss\text{ eq. (3)}}$	Equivalent Output Capacitance	$V_{GS} = 0\text{V}$ , $V_{DS} = 0\text{V}$ to $720\text{V}$		70		pF

### SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 450\text{ V}$ , $I_D = 3\text{ A}$ $R_G = 4.7\Omega$ , $V_{GS} = 10\text{ V}$ (Resistive Load see, Figure 3)		17 20		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 720\text{ V}$ , $I_D = 5.8\text{ A}$ , $V_{GS} = 10\text{V}$		46.5 8.5 25		nC nC nC

### SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 450\text{ V}$ , $I_D = 3\text{ A}$ $R_G = 4.7\Omega$ , $V_{GS} = 10\text{ V}$ (Resistive Load see, Figure 3)		45 20		ns ns
$t_{r(Voff)}$ $t_f$ $t_c$	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 720\text{V}$ , $I_D = 5.8\text{ A}$ , $R_G = 4.7\Omega$ , $V_{GS} = 10\text{V}$ (Inductive Load see, Figure 5)		11 12 20		ns ns ns

### SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM(2)}$	Source-drain Current Source-drain Current (pulsed)				5.8 23.2	A A
$V_{SD}(1)$	Forward On Voltage	$I_{SD} = 5.8\text{ A}$ , $V_{GS} = 0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 5.8\text{ A}$ , $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 36\text{V}$ , $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		840 5880 14		ns nC A

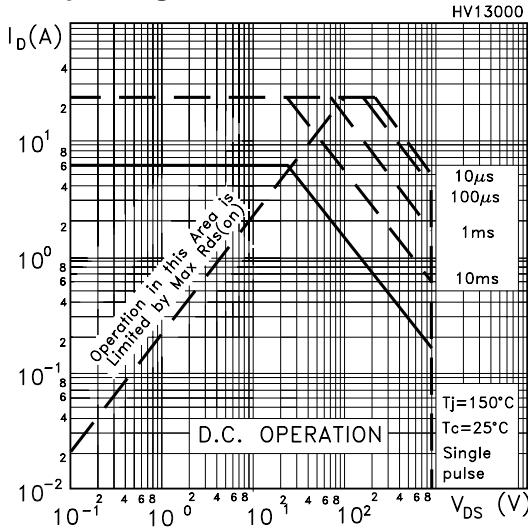
Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

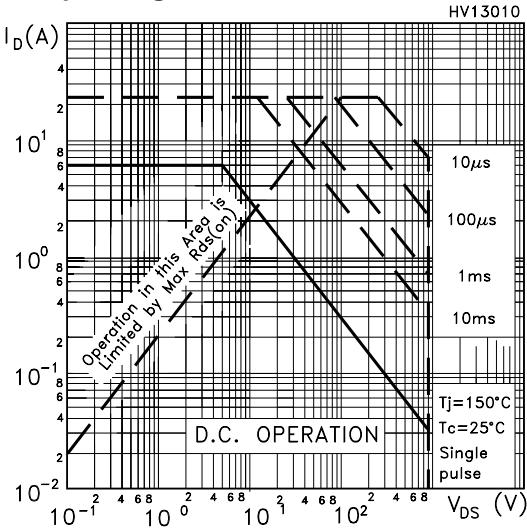
3.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

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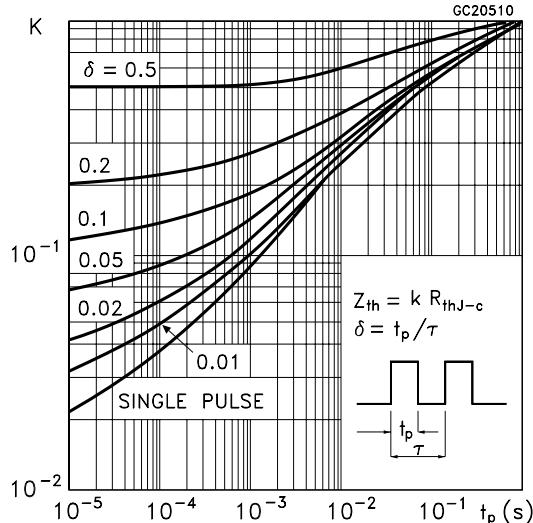
### Safe Operating Area For TO-220/D2PAK



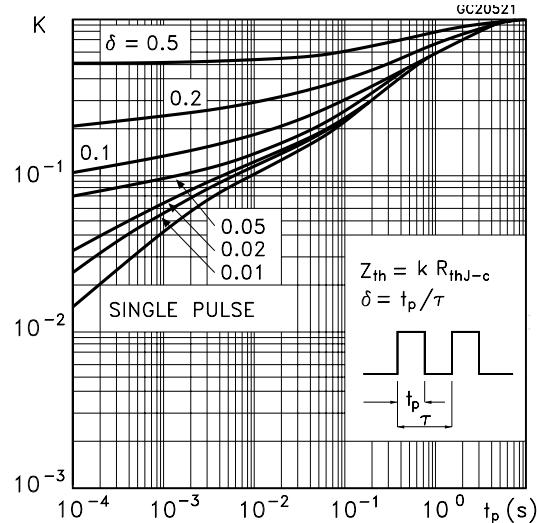
### Safe Operating Area For TO-220FP



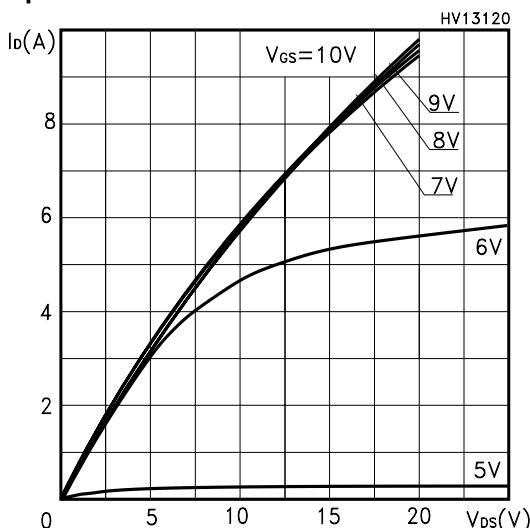
### Thermal Impedance For TO-220/D2PAK



### Thermal Impedance For TO-220FP



### Output Characteristics



### Transfer Characteristics

