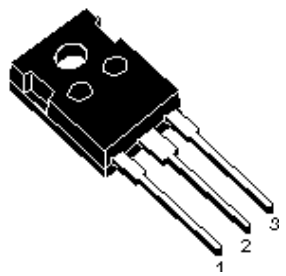
STW7NC90Z

N-CHANNEL 900V - 1.55Ω - 6A TO-247
Zener-Protected PowerMESH™III MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STW7NC90Z	900 V	< 1.9 Ω	6 A

- TYPICAL R_{DS}(on) = 1.55Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- GATE-TO-SOURCE ZENER DIODES
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED



TO-247

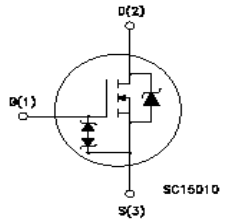
DESCRIPTION

The third generation of MESH OVERLAY™ Power MOSFETs for very high voltage exhibits unsurpassed on-resistance per unit area while integrating back-to-back Zener diodes between gate and source. Such arrangement gives extra ESD capability with higher ruggedness performance as requested by a large variety of single-switch applications.

APPLICATIONS

- SINGLE-ENDED SMPS IN MONITORS, COMPUTER AND INDUSTRIAL APPLICATION
- WELDING EQUIPMENT

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	900	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	900	V
V_{GS}	Gate- source Voltage	±25	V
I_D	Drain Current (continuos) at T_C = 25°C	6	A
I_D	Drain Current (continuos) at T_C = 100°C	3.8	A
I_{DM} (•)	Drain Current (pulsed)	24	A
P_{TOT}	Total Dissipation at T_C = 25°C	160	W
	Derating Factor	1.28	W/°C
I_{GS}	Gate-source Current (DC)	±50	mA
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=15KΩ)	3	KV
dv/dt(1)	Peak Diode Recovery voltage slope	3	V/ns
T_{stg}	Storage Temperature	–65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area

(*) Limited by maximum temperature allowed

(1)I_{SD} ≤6A, di/dt ≤100A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}.

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.78	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	30	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	6	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	315	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	900			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = 1 mA, V_{GS} = 0		1		V/°C
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±20V			±10	µA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 3A		1.55	1.9	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D =3A		5.7		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		2290		pF
C_{oss}	Output Capacitance			150		pF
C_{rss}	Reverse Transfer Capacitance			15		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON (RESISTIVE LOAD)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 450V, I_D = 3A R_G = 4.7Ω V_{GS} = 10V (see test circuit, Figure 3)		30		ns
t_r	Rise Time			12		ns
Q_g	Total Gate Charge	V_{DD} = 720V, I_D = 6 A, V_{GS} = 10V		42	58.8	nC
Q_{gs}	Gate-Source Charge			13		nC
Q_{gd}	Gate-Drain Charge			15		nC

SWITCHING OFF (INDUCTIVE LOAD)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 720V, I_D = 6 A, R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 5)		10		ns
t_f	Fall Time			11		ns
t_c	Cross-over Time			14		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				6	A
I_{SDM} (2)	Source-drain Current (pulsed)				24	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 6 A, V_{GS} = 0			1.6	V
t_{rr}	Reverse Recovery Time	I_{SD} = 6 A, di/dt = 100A/µs, V_{DD} = 40 V, T_j = 150°C (see test circuit, Figure 5)		680		ns
Q_{rr}	Reverse Recovery Charge			7.14		µC
I_{RRM}	Reverse Recovery Current			21		A

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	Igs=± 1mA (Open Drain)	25			V
αT	Voltage Thermal Coefficient	T=25°C Note(3)		1.3		10^{-4}/°C
Rz	Dynamic Resistance	I_{GS} = 50 mA		90		Ω

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. $\Delta V_{BV} = \alpha T\ (25°\text{-}T)\ BV_{GSO}(25°)$

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to souce. In this respect the 25V Zener voltage is appropiate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.