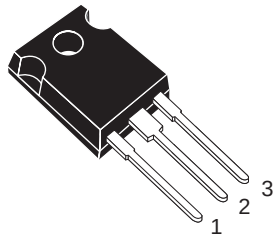
STW77N65M5

N-channel 650 V, 0.033 Ω, 69 A, MDmesh™ V Power MOSFET
TO-247

Features

Order code	V_{DSS} @$T_{jmax.}$	$R_{DS(on)}$ max.	I_D
STW77N65M5	710 V	< 0.038 Ω	69 A

- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested



TO-247

Application

Switching applications

Description

This device is a N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram

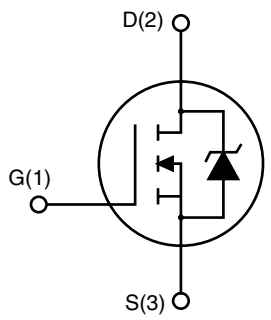


Table 1. Device summary

Order code	Marking	Package	Packaging
STW77N65M5	77N65M5	TO-247	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	25	V
I_D	Drain current (continuous) at T_C = 25 °C	69	A
I_D	Drain current (continuous) at T_C = 100 °C	41.5	A
I_{DM} (1)	Drain current (pulsed)	276	A
P_{TOT}	Total dissipation at T_C = 25 °C	400	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	15	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	2000	mJ
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq$ 69 A, di/dt = 400 A/µs, peak $V_{DS} < V_{(BR)DSS}$, V_{DD} = 400 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.31	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	50	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 34.5 A		0.033	0.038	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	9800 200 6	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 520 V	-	590	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related	V_{GS} = 0, V_{DS} = 0 to 520 V	-	194	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.2	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 34.5 A, V_{GS} = 10 V	-	185 45 65	-	nC nC nC

1. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
2. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	V_{DD} = 400 V, I_D = 40 A,	-	160	-	ns
$t_{r(V)}$	Voltage rise time	R_G = 4.7 Ω, V_{GS} = 10 V		22		ns
$t_{f(i)}$	Current fall time			20		ns
$t_{c(off)}$	Crossing time			40		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		69	A
I_{SDM} (1)	Source-drain current (pulsed)				276	A
V_{SD} (2)	Forward on voltage	I_{SD} = 69 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 69 A,	-	570		ns
Q_{rr}	Reverse recovery charge	di/dt = 100 A/µs		14		µC
I_{RRM}	Reverse recovery current	V_{DD} = 100 V (see)		48		A
t_{rr}	Reverse recovery time	I_{SD} = 69 A,	-	700		ns
Q_{rr}	Reverse recovery charge	di/dt = 100 A/µs		20		µC
I_{RRM}	Reverse recovery current	V = 100 V, T = 150 °C		58		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

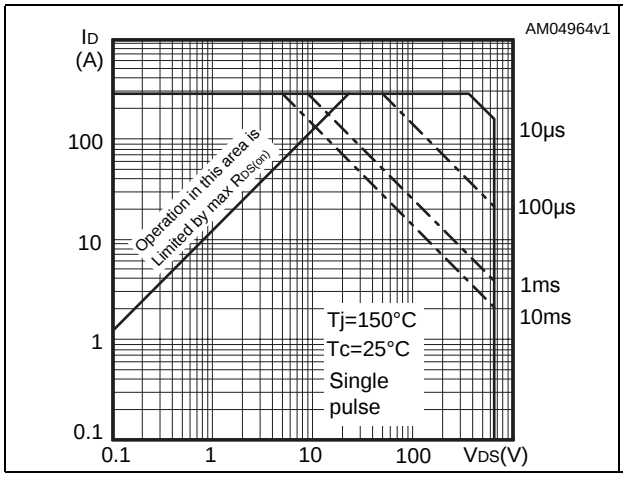


Figure 3. Thermal impedance

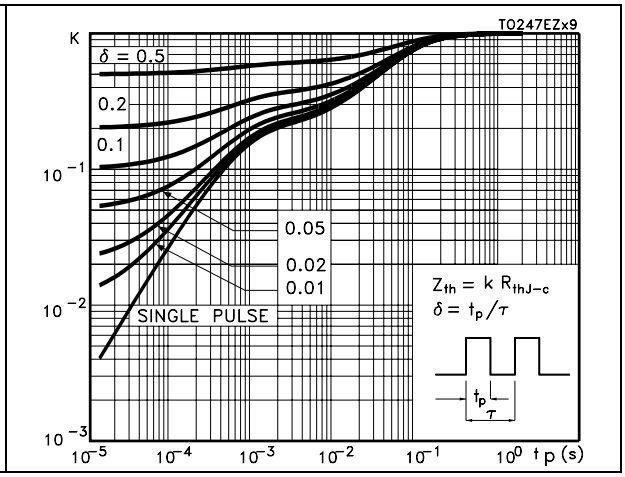


Figure 4. Output characteristics

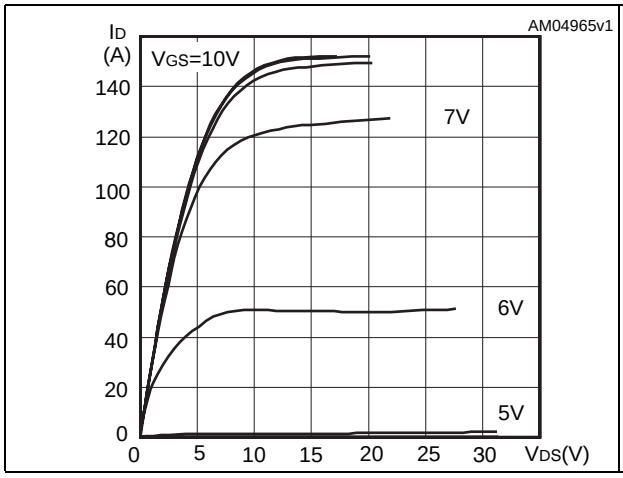


Figure 5. Transfer characteristics

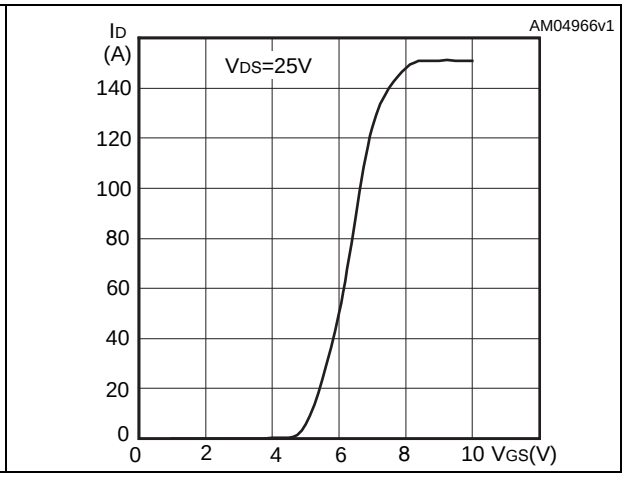


Figure 6. Gate charge vs gate-source voltage

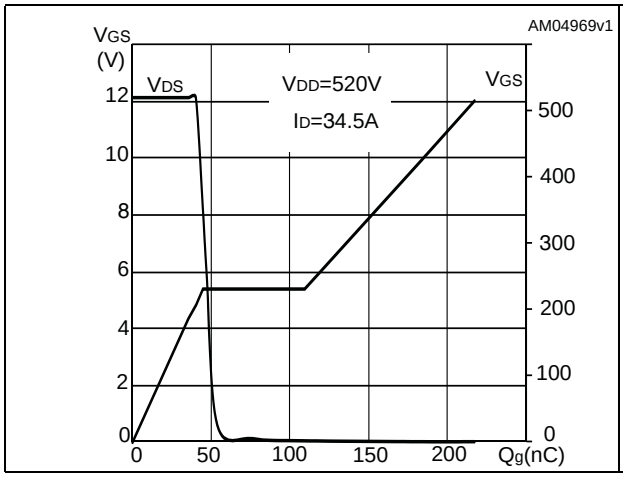


Figure 7. Static drain-source on resistance