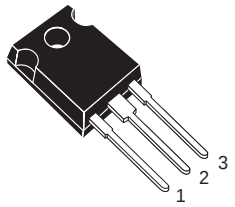
# STW60NM50N

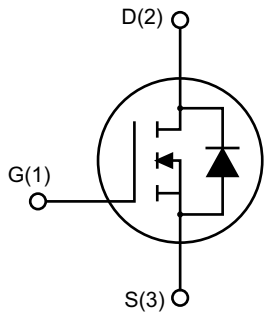
## N-channel 500 V, 0.035 Ω, 68 A, MDmesh™ II Power MOSFET in a TO-247 package

**Datasheet - production data**




**TO-247**

**Figure 1. Internal schematic diagram**




## Features

| Order code | $V_{DSS}$ (@$T_{jmax}$) | $R_{DS(on)\ max}$ | $I_D$ |
|---|---|---|---|
| STW60NM50N | 550 V | <0.043 Ω | 68 A |

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Applications

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

**Table 1. Device summary**

| Order codes | Marking | Packages | Packaging |
|---|---|---|---|
| STW60NM50N | 60NM50N | TO-247 | Tube |

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate- source voltage | ±25 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 68 | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 43 | A |
| $I_{DM}$ (1) | Drain current (pulsed) | 272 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 446 | W |
| dv/dt (2) | Peak diode recovery voltage slope | 15 | V/ns |
| $T_{stg}$ | Storage temperature | –55 to 150 | °C |
| $T_j$ | Max. operating junction temperature | 150 | °C |

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq$ 68 A, di/dt $\leq$ 400 A/µs, $V_{DD}$ =80% $V_{(BR)DSS}$

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 0.28 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient max | 50 | °C/W |

**Table 4. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AS}$ | Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{j\ Max}$) | 11 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting Tj=25 °C, $I_D$=$I_{AS}$, $V_{DD}$=50 V) | 551 | mJ |

# 2 Electrical characteristics

($T_{CASE}$=25 °C unless otherwise specified)

**Table 5. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0, $I_D$ = 1 mA | 500 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0, $V_{DS}$ = 500 V<br>$V_{GS}$ = 0, $V_{DS}$ = 500 V, $T_j$ = 125 °C | | | 1<br>100 | µA |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0, $V_{GS}$ = ± 20 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 34 A | | 0.035 | 0.043 | Ω |

**Table 6. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 | - | 5790 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 365 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 14 | - | pF |
| $C_{oss\ eq.}$ (1) | Equivalent output capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 0V to 480 V | - | 1008 | - | pF |
| $Q_g$ | Total gate charge | $V_{DD}$ = 480 V, $I_D$ = 68 A, $V_{GS}$ = 10 V | - | 178 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 28 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 95 | - | nC |
| $R_g$ | Gate input resistance | f=1 MHz gate DC bias=0<br>Test signal level = 20 mV<br>open drain | - | 2 | - | Ω |

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DS}$

**Table 7. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ =300 V, $I_D$ = 32.5 A<br>$R_G$ = 4.7 Ω $V_{GS}$ = 10 V | - | 206 | - | ns |
| $t_r$ | Rise time | | - | 36 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 40 | - | ns |
| $t_f$ | Fall time | | - | 27.5 | - | ns |

**Table 8. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current<br>Source-drain current (pulsed) | | - | | 68 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | - | | 272 | A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 68 A, $V_{GS}$ = 0 | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 68 A, di/dt = 100 A/µs<br>$V_{DD}$ = 100 V | - | 476 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 10.5 | | nC |
| $I_{RRM}$ | Reverse recovery current | | - | 44 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 68 A, di/dt = 100 A/µs<br>$V_{DD}$ = 100 V, $T_j$ = 150 °C | - | 586 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 15 | | nC |
| $I_{RRM}$ | Reverse recovery current | | - | 51 | | A |

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

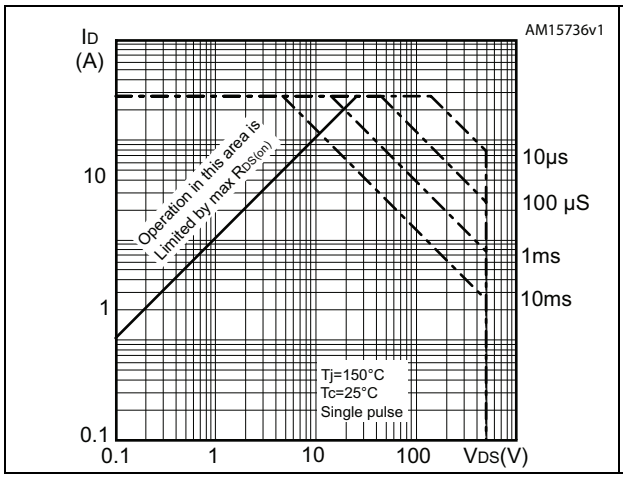



**Figure 3. Thermal impedance**

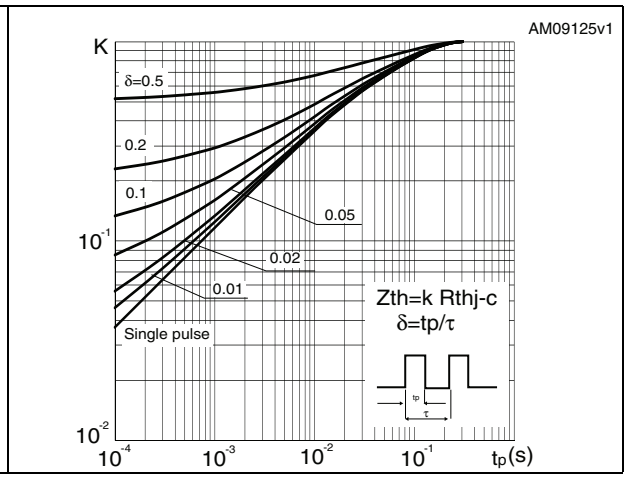



**Figure 4. Output characteristics**

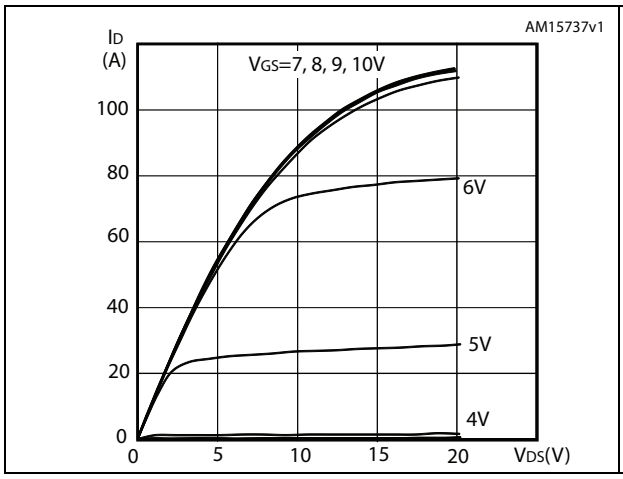



**Figure 5. Transfer characteristics**

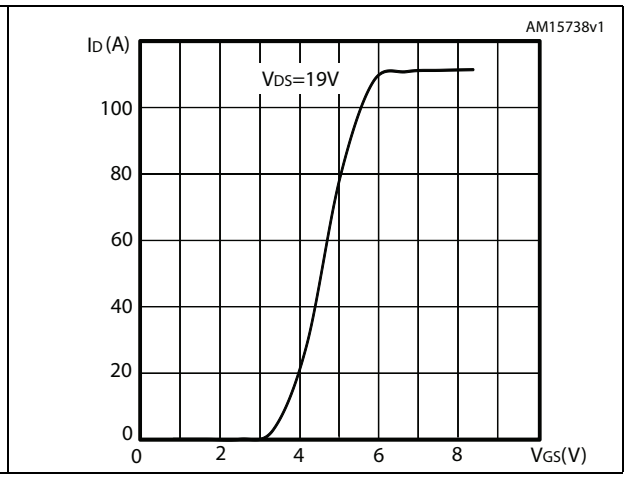



**Figure 6. Normalized $V_{(BR)DSS}$ vs temperature**

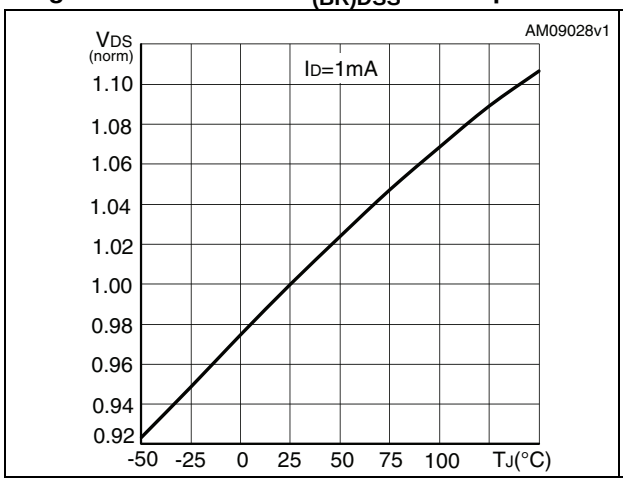



**Figure 7. Static drain-source on-resistance**