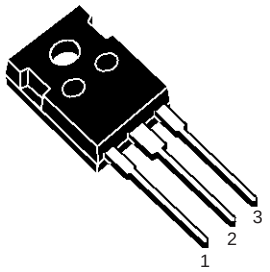
STW5NB90

N - CHANNEL 900V - 2.3Ω - 5.6A - TO-247
PowerMESH™ MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STW5NB90	900 V	< 2.5 Ω	5.6 A

- TYPICAL $R_{DS(on)}$ = 2.3 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED



TO-247

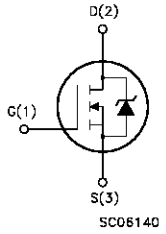
DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest $R_{DS(on)}$ per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

APPLICATIONS

- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE
- HIGH CURRENT, HIGH SPEED SWITCHING

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	900	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	900	V
V_{GS}	Gate-source Voltage	± 30	V
I_D	Drain Current (continuous) at T_c = 25 °C	5.6	A
I_D	Drain Current (continuous) at T_c = 100 °C	3.3	A
I_{DM}(•)	Drain Current (pulsed)	22.4	A
P_{tot}	Total Dissipation at T_c = 25 °C	160	W
	Derating Factor	1.28	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	4	V/ns
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

(1) $I_{SD} \leq$ 5A, di/dt ≤ 200 A/µs, $V_{DD} \leq V_{(BR)DSS}$, Tj ≤ T_{JMAX}

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	0.78	$^oC/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	30	oC/W
$R_{thc-sink}$	Thermal Resistance Case-sink	Typ	0.1	$^oC/W$
T_l	Maximum Lead Temperature For Soldering Purpose		300	^oC

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	5.6	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 ^oC, $I_D = I_{AR}$, V_{DD} = 50 V)	284	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 ^oC unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	900			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_c = 125 ^oC			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 30 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V I_D =2.5 A		2.3	2.5	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ V_{GS} = 10 V	5.6			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ I_D = 2.5 A	2.5	4.1		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		1250 128 13		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 450 V I_D = 2.5 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 3)		18 9		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 720 V I_D =5 A V_{GS} = 10 V R_G = 4.7 Ω V_{GS} = 10 V		33 10 13	47	nC nC nC

SWITCHING OFF

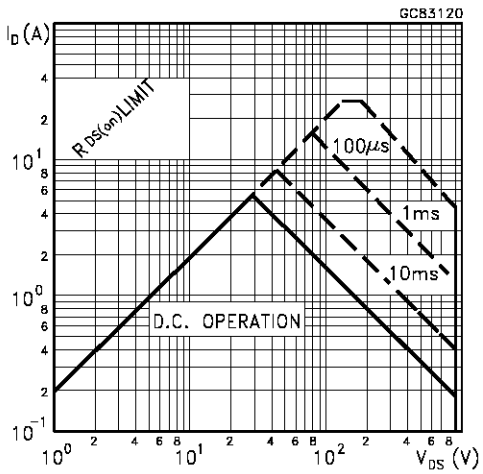
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 720 V I_D = 5 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 5)		13 10 17		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				5.6 22.4	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 5 A V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 5 A di/dt = 100 A/µs V_{DD} = 100 V T_j = 150 °C (see test circuit, figure 5)		700 5.4 15.5		ns µC A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

Safe Operating Area



Thermal Impedance