STB57N65M5, STF57N65M5, STI57N65M5, STP57N65M5

N-channel 650 V, 0.056 Ω typ., 42 A MDmesh™ V Power MOSFET in I²PAK, TO-220, TO-220FP and D²PAK packages

Datasheet — production data

Features

Order codes	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STB57N65M5 STF57N65M5 STI57N65M5 STP57N65M5	710 V	< 0.063 Ω	42 A

- Worldwide best $R_{DS(on)}$*area amongst the silicon based devices
- Higher V_{DSS} rating, high dv/dt capability
- Excellent switching performance
- Easy to drive, 100% avalanche tested

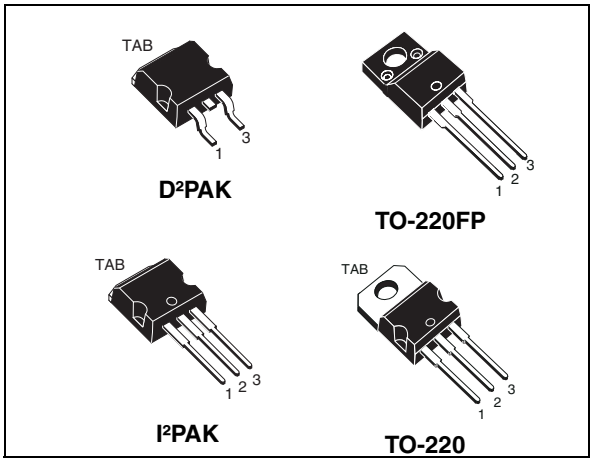
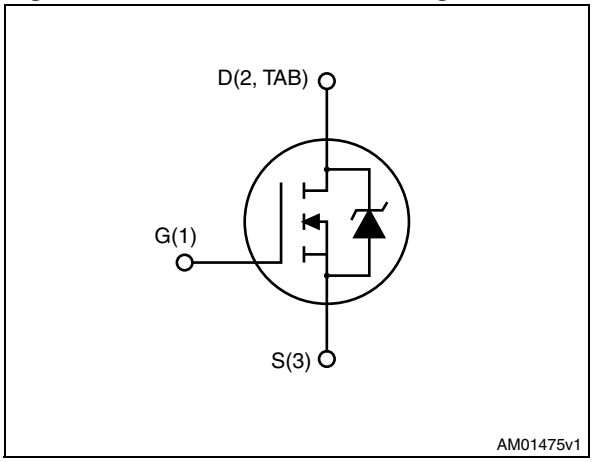


Figure 1. Internal schematic diagram



Applications

- Switching applications

Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STB57N65M5	57N65M5	D²PAK	Tape and reel
STF57N65M5		TO-220FP	Tube
STI57N65M5		I²PAK	Tube
STP57N65M5		TO-220	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, D²PAK, I²PAK	TO-220FP	
V_{GS}	Gate- source voltage	± 25		V
I_D	Drain current (continuous) at T_C = 25 °C	42	42 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	26.5	26.5 (1)	A
I_{DM} (2)	Drain current (pulsed)	168	168 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	250	40	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	11		A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}, V_{DD} = 50V)	960		mJ
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; Tc = 25 °C)		2500	V
T_{stg}	Storage temperature	-55 to 150		°C
T_j	Max. operating junction temperature	150		°C

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 42$ A, di/dt $\leq$ 400 A/µs, $V_{Peak} < V_{(BR)DSS}$, V_{DD} = 400 V

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		D²PAK	I²PAK	TO-220	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	0.50			3.1	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max		62.5		62.5	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max(1)	30				°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 650 V V_{DS} = 650 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 21 A		0.056	0.063	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	4200 115 9	-	pF pF pF
$C_{o(er)}$(1)	Equivalent output capacitance energy related	V_{GS} = 0, V_{DS} = 0 to 80% $V_{(BR)DSS}$	-	93	-	pF
$C_{o(tr)}$(2)	Equivalent output capacitance time related	V_{GS} = 0, V_{DS} = 0 to 80% $V_{(BR)DSS}$	-	303	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.3	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 21 A, V_{GS} = 10 V	-	98 23 40	-	nC nC nC

1. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
2. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$ $t_{r(V)}$ $t_{f(i)}$ $t_{c(off)}$	Voltage delay time Voltage rise time Current fall time Crossing time	V_{DD} = 400 V, I_D = 28 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	73 15 12 19	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		42 168	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 42 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 42 A, di/dt = 100 A/µs V_{DD} = 100 V (see	-	418 8 40		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 42 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C	-	528 12 44		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK, I²PAK and TO-220

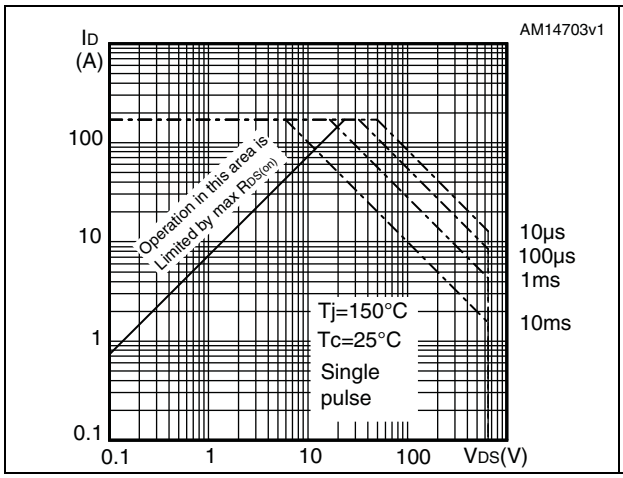


Figure 3. Thermal impedance for D²PAK, I²PAK and TO-220

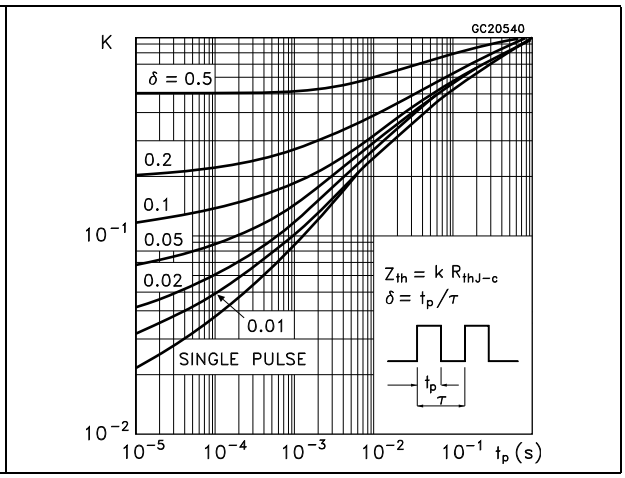


Figure 4. Safe operating area for TO-220FP

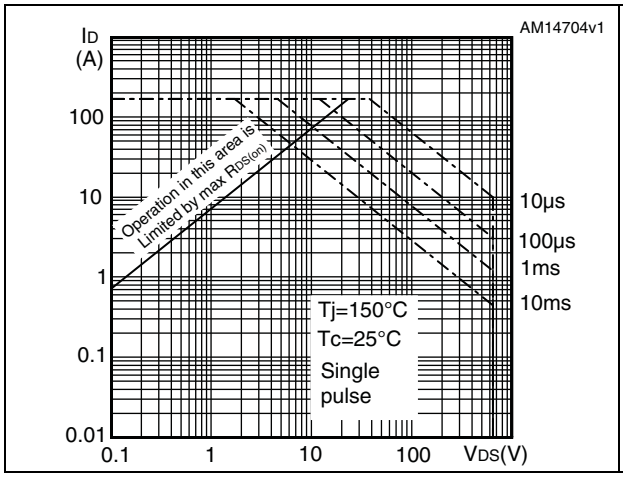


Figure 5. Thermal impedance for TO-220FP

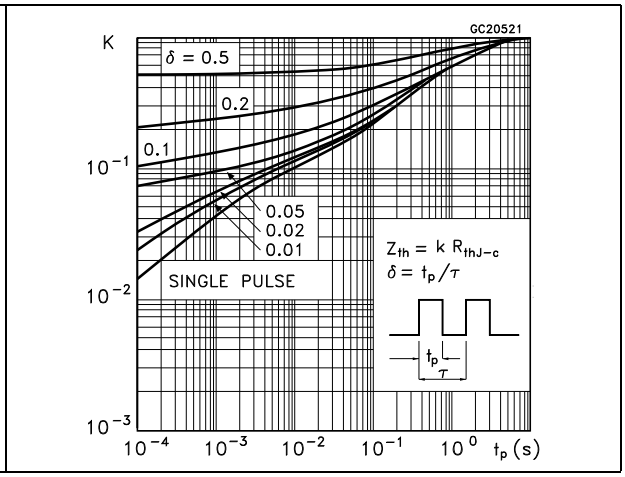


Figure 6. Output characteristics

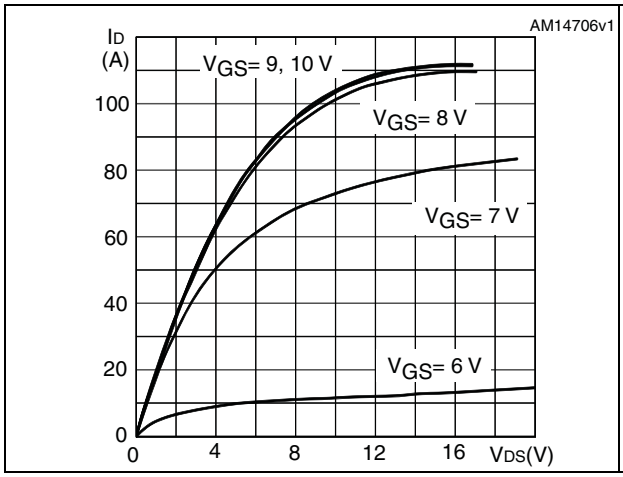


Figure 7. Transfer characteristics

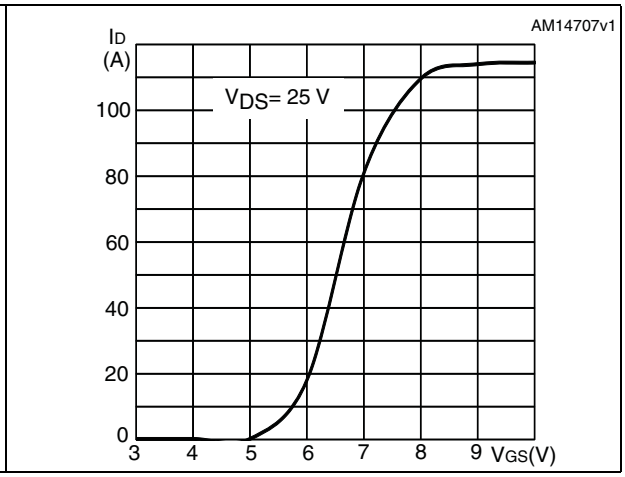


Figure 8. Gate charge vs gate-source voltage

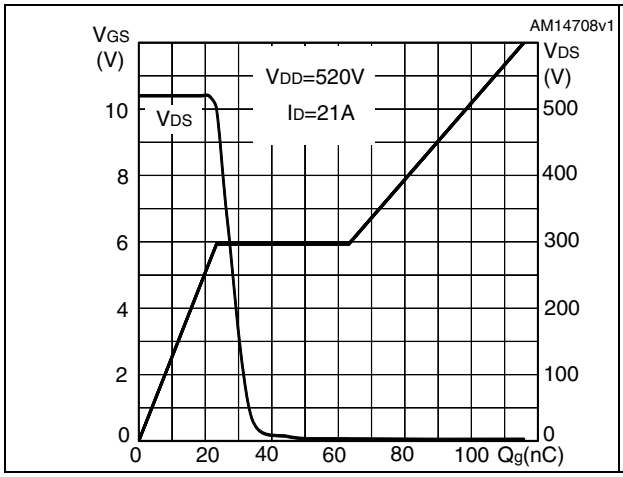


Figure 9. Static drain-source on-resistance

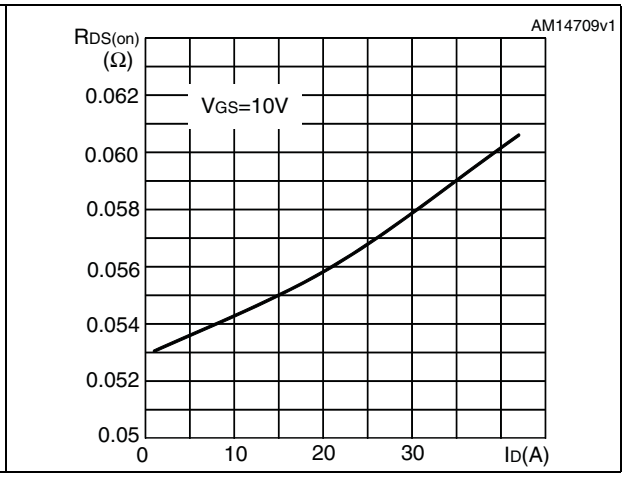


Figure 10. Capacitance variations

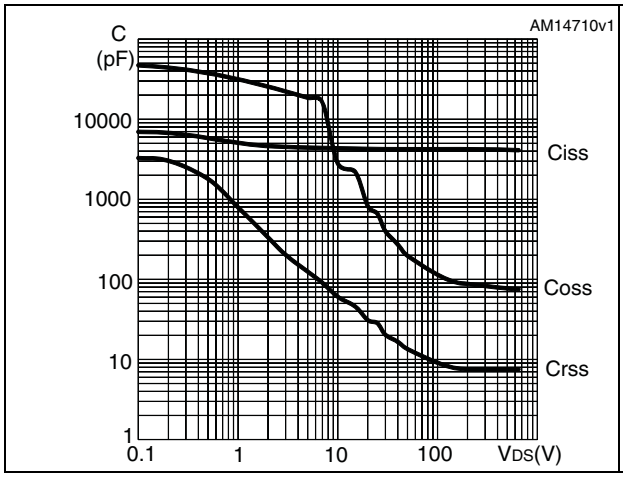


Figure 11. Output capacitance stored energy

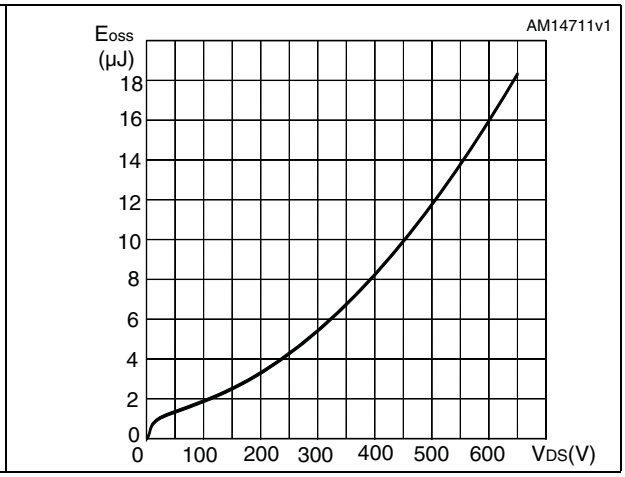


Figure 12. Normalized gate threshold voltage vs temperature

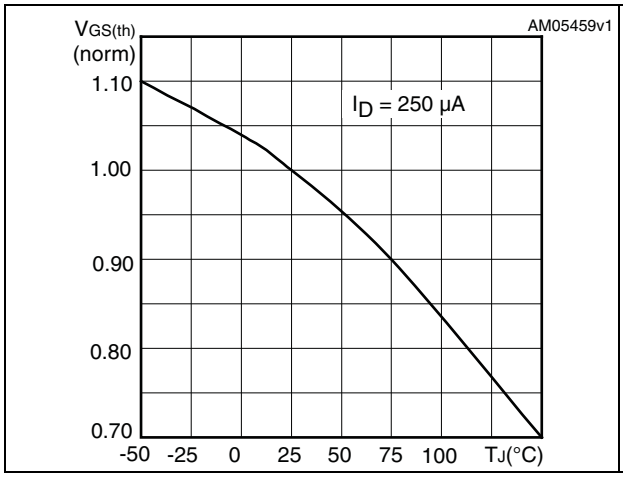


Figure 13. Normalized on-resistance vs temperature