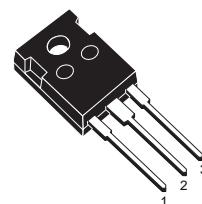


**N-CHANNEL 500V - 0.065Ω - 45A TO-247**  
**MDmesh™ Power MOSFET**
**ADVANCED DATA**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	R <sub>ds(on)*Q<sub>g</sub></sub>	I <sub>D</sub>
STW47NM50	500V	< 0.085Ω	5.6 Ω*nC	45 A

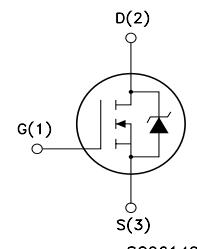
- TYPICAL R<sub>DS(on)</sub> = 0.065Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS


**TO-247**
**DESCRIPTION**

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

**APPLICATIONS**

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

**INTERNAL SCHEMATIC DIAGRAM**

**SC06140**
**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	500	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	500	V
V <sub>GS</sub>	Gate- source Voltage	±30	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	45	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	28.4	A
I <sub>DM (•)</sub>	Drain Current (pulsed)	180	A
P <sub>TOT</sub>	Total Dissipation at T <sub>c</sub> = 25°C	417	W
	Derating Factor	2.08	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	15	V/ns
T <sub>stg</sub>	Storage Temperature	-65 to 150	°C
T <sub>j</sub>	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 45A, di/dt ≤ 400A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

## STW47NM50

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### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	0.3	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	30	°C/W
T <sub>L</sub>	Maximum Lead Temperature For Soldering Purpose		300	°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	20	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 35 V)	810	mJ

### ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	500			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			10 100	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±30 V			±100	nA

### ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3	4	5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 22.5 A		0.065	0.085	Ω

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , I <sub>D</sub> = 22.5A		20		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		3700		pF
C <sub>oss</sub>	Output Capacitance			610		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			50		pF
C <sub>oss eq.</sub> (2)	Equivalent Output Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 400V		325		pF
R <sub>G</sub>	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.7		Ω

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

2. C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>.

**ELECTRICAL CHARACTERISTICS (CONTINUED)**  
**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 250V, I_D = 22.5A$		40		ns
$t_r$	Rise Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		35		ns
$Q_g$	Total Gate Charge	$V_{DD} = 400V, I_D = 45A, V_{GS} = 10V$		87	117	nC
$Q_{gs}$	Gate-Source Charge			23		nC
$Q_{gd}$	Gate-Drain Charge			42		nC

**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(loff)}$	Off-voltage Rise Time	$V_{DD} = 400V, I_D = 45A, R_G = 4.7\Omega, V_{GS} = 10V$		18		ns
$t_f$	Fall Time			23		ns
$t_c$	Cross-over Time			44		ns

**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				45	A
$I_{SDM}(2)$	Source-drain Current (pulsed)				180	A
$V_{SD}(1)$	Forward On Voltage	$I_{SD} = 45A, V_{GS} = 0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 40A, di/dt = 100A/\mu s, V_{DD} = 100V, T_j = 25^\circ C$ (see test circuit, Figure 5)		520 7.8 30		ns $\mu C$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 40A, di/dt = 100A/\mu s, V_{DD} = 100V, T_j = 150^\circ C$ (see test circuit, Figure 5)		680 11.2 33		ns $\mu C$ A

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.