

N-channel 650 V, 0.070 Ω , 33 A MDmesh™ V Power MOSFET
in I²PAK, TO-220, TO-220FP, D²PAK and TO-247

Features

Type	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STB42N65M5	710 V	< 0.079 Ω	33 A
STF42N65M5	710 V	< 0.079 Ω	33 A ⁽¹⁾
STI42N65M5	710 V	< 0.079 Ω	33 A
STP42N65M5	710 V	< 0.079 Ω	33 A
STW42N65M5	710 V	< 0.079 Ω	33 A

1. Limited only by maximum temperature allowed

- TO-220 worldwide best $R_{DS(on)}$
- Higher V_{DSS} rating
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

Application

- Switching applications

Description

MDmesh™ V is a revolutionary Power MOSFET technology based on an innovative proprietary vertical process, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiencies.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB42N65M5	42N65M5	D ² PAK	Tape and reel
STF42N65M5	42N65M5	TO-220FP	Tube
STI42N65M5	42N65M5	I ² PAK	Tube
STP42N65M5	42N65M5	TO-220	Tube
STW42N65M5	42N65M5	TO-247	Tube

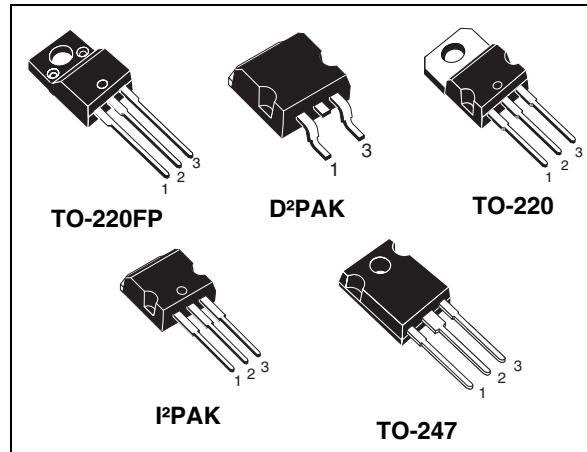
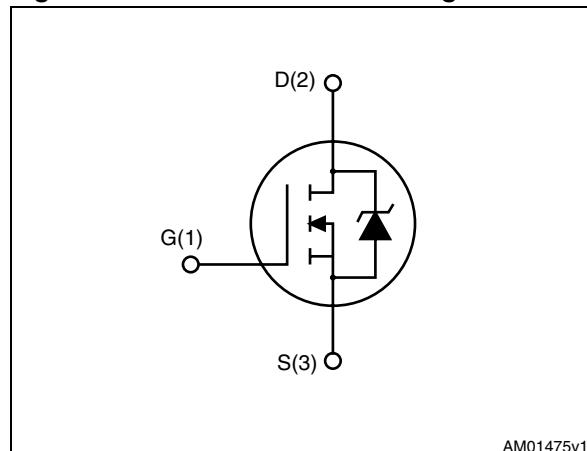


Figure 1. Internal schematic diagram



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, TO-247 D ² PAK, I ² PAK	TO-220FP	
V_{GS}	Gate- source voltage	± 25		V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	33	33 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	20.8	20.8 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	132	132 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	190	40	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	11		A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{V}$)	950		mJ
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_c = 25^\circ\text{C}$)	--	2500	V
T_{stg}	Storage temperature	-55 to 150		°C
T_j	Max. operating junction temperature	150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 33\text{ A}$, $dI/dt \leq 400\text{ A}/\mu\text{s}$, $V_{Peak} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value					Unit
		D ² PAK	I ² PAK	TO-220	TO-247	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	0.66		3.1		°C/W	
$R_{thj-amb}$	Thermal resistance junction-ambient max	--	62.5		50	62.5	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max	30	--	--	--	--	°C/W
T_I	Maximum lead temperature for soldering purpose	300					°C

2 Electrical characteristics

($T_C = 25^\circ\text{C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}, T_C = 125^\circ\text{C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25 \text{ V}$			100	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	3	4	5	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 16.5 \text{ A}$		0.070	0.079	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance			4650		pF
C_{oss}	Output capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz},$ $V_{GS} = 0$	-	110	-	pF
C_{rss}	Reverse transfer capacitance			3.2		pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0, V_{DS} = 0 \text{ to } 80\%$ $V_{(\text{BR})\text{DSS}}$	-	100	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related	$V_{GS} = 0, V_{DS} = 0 \text{ to } 80\%$ $V_{(\text{BR})\text{DSS}}$	-	285	-	pF
R_G	Intrinsic gate resistance	$f = 1 \text{ MHz open drain}$	-	1.1	-	Ω
Q_g	Total gate charge	$V_{DD} = 520 \text{ V}, I_D = 16.5 \text{ A},$ $V_{GS} = 10 \text{ V}$		100		nC
Q_{gs}	Gate-source charge		-	26	-	nC
Q_{gd}	Gate-drain charge			38		nC

1. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}
2. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400 \text{ V}$, $I_D = 20 \text{ A}$, $R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$	-	61	ns	ns
t_r	Rise time			24		
$t_{d(off)}$	Turn-off-delay time			65	ns	ns
t_f	Fall time			13		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current		-	33 132	A A	A
	Source-drain current (pulsed)					
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 33 \text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 33 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}$ (see)	-	400 7 35		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 33 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 100 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$	-	532 10 38		ns μC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D²PAK, I²PAK

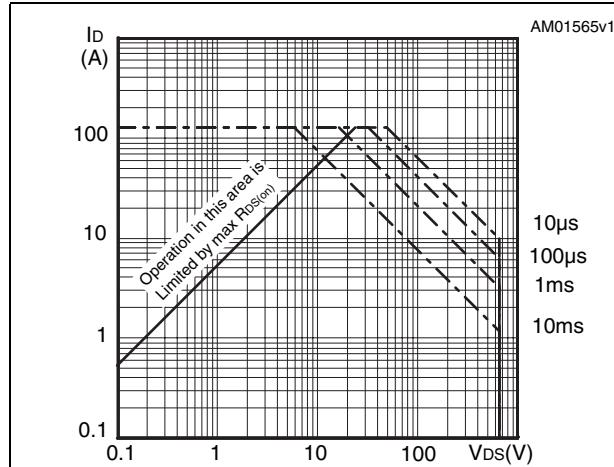


Figure 3. Thermal impedance for TO-220, D²PAK, I²PAK

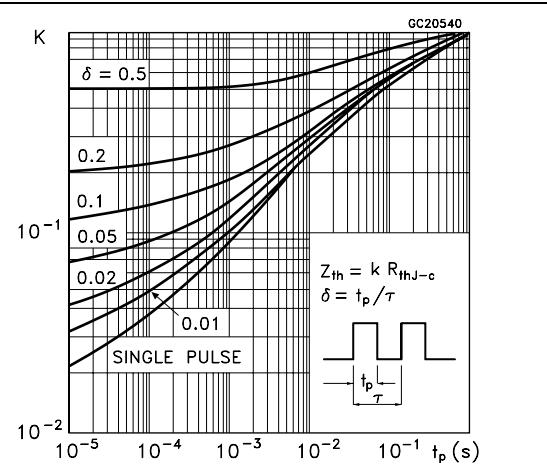


Figure 4. Safe operating area for TO-247

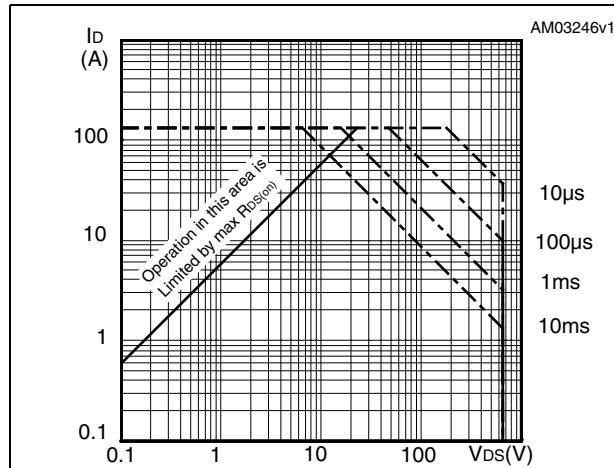


Figure 5. Thermal impedance for TO-247

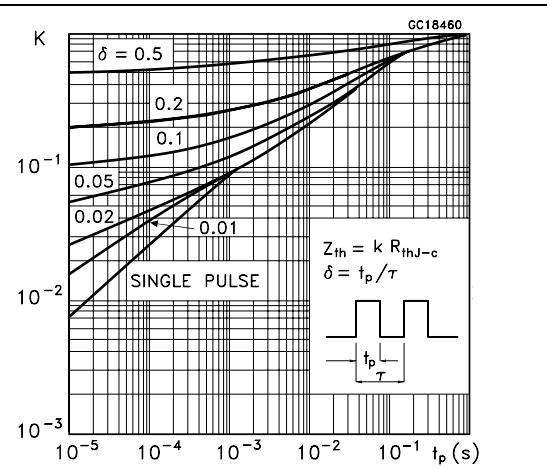


Figure 6. Safe operating area for TO-220FP

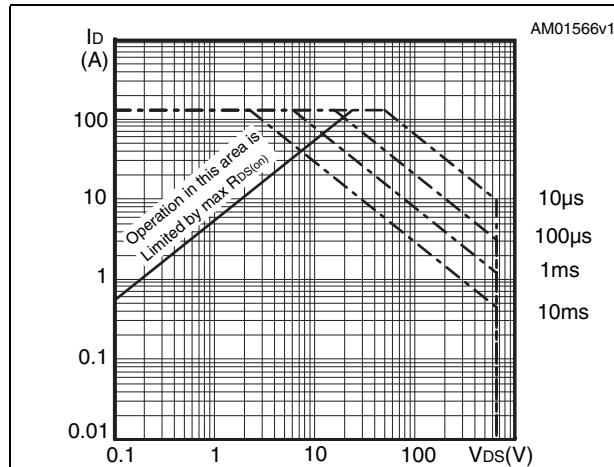


Figure 7. Thermal impedance for TO-220FP

