

STP40NF20 - STF40NF20 STB40NF20 - STW40NF20

N-channel 200V - 0.038Ω -40A- D²PAK/TO-220/TO-220FP/TO-247
Low gate charge STripFET™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)}	I _D	P _W
STB40NF20	200V	<0.045Ω	40A	160W
STP40NF20	200V	<0.045Ω	40A	160W
STF40NF20	200V	<0.045Ω	40A	40W
STW40NF20	200V	<0.045Ω	40A	160W

- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability
- Excellent figure of merit (R_{DS}*Q_g)
- 100% avalanche tested

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters.

Applications

- Switching application

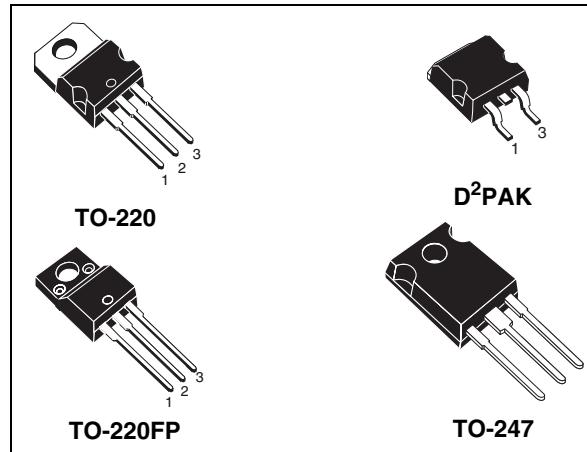


Figure 1. Internal schematic diagram

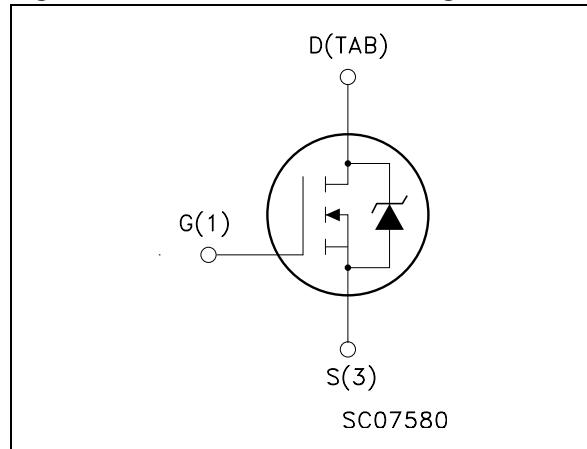


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB40NF20	40NF20	D ² PAK	Tape & reel
STP40NF20	40NF20	TO-220	Tube
STF40NF20	40NF20	TO-220FP	Tube
STW40NF20	40NF20	TO-247	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220 D ² PAK TO-247	TO-220FP	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	200		V
V_{GS}	Gate- source voltage		± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	40		A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	25		A
$I_{DM}^{(2)}$	Drain current (pulsed)	160		A
P_{tot}	Total dissipation at $T_C = 25^\circ\text{C}$	160	40	W
	Derating Factor	1.28	0.32	W/ $^\circ\text{C}$
dv/dt ⁽³⁾	Peak diode recovery voltage slope	12		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{s}; T_c = 25^\circ\text{C}$)	--	2500	V
T_{stg}	Storage temperature	-55 to 150		$^\circ\text{C}$
T_j	Max. operating junction temperature			

1. Value limited by wire bonding
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 40\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

Table 2. Thermal data

Symbol	Parameter	TO-220 D ² PAK	TO-247	TO-220FP	Unit
R _{thj-case}	Thermal resistance junction-case max	0.78		3.1	$^\circ\text{C/W}$
R _{thj-amb}	Thermal resistance junction-ambient max	62.5	50	62.5	$^\circ\text{C/W}$
T_j	Maximum lead temperature for soldering purpose ⁽¹⁾		300		$^\circ\text{C}$

1. for 10 sec. 1.6mm from case

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	40	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{V}$)	230	mJ

2 Electrical characteristics

($T_{CASE}=25^\circ\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{mA}$, $V_{GS} = 0$	200			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max ratings}$ $V_{DS} = \text{max ratings}@125^\circ\text{C}$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 100	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2	3	4	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 20\text{A}$		0.038	0.045	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$, $I_D = 20\text{A}$		30		s
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		2500 510 78		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 100\text{V}$, $I_D = 20\text{A}$ $R_G = 4.7\Omega$ $V_{GS} = 10\text{V}$		20 44 74 22		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 160\text{V}$, $I_D = 40\text{A}$, $V_{GS} = 10\text{V}$		75 13.2 35.5		nC nC nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				40 160	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20A, V_{GS} = 0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 20A,$ $dI/dt = 100A/\mu s,$ $V_{DD} = 25V$		192 922 9.6		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 20A,$ $dI/dt = 100A/\mu s,$ $V_{DD} = 25V, T_j = 150^\circ C$		242 1440 11.9		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220/D²PAK

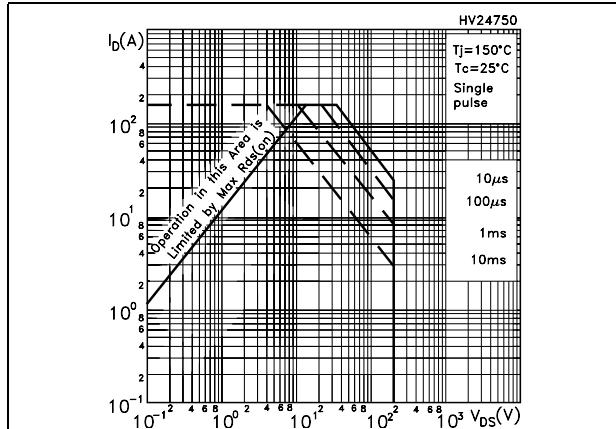


Figure 4. Safe operating area for TO-247

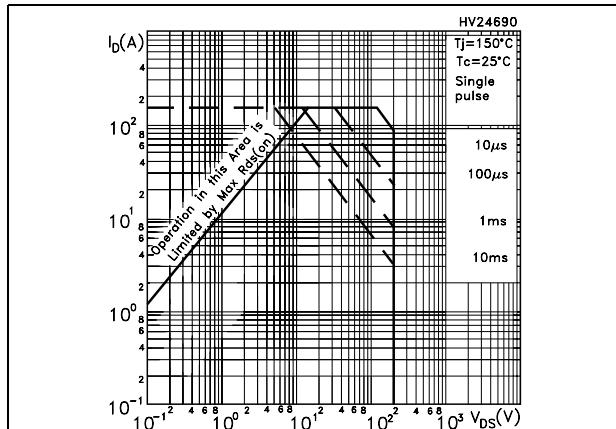


Figure 6. Safe operating area for TO-220FP

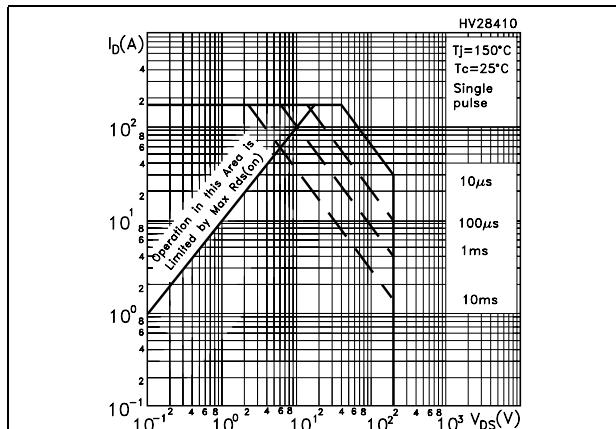


Figure 3. Thermal impedance area for TO-220/D²PAK

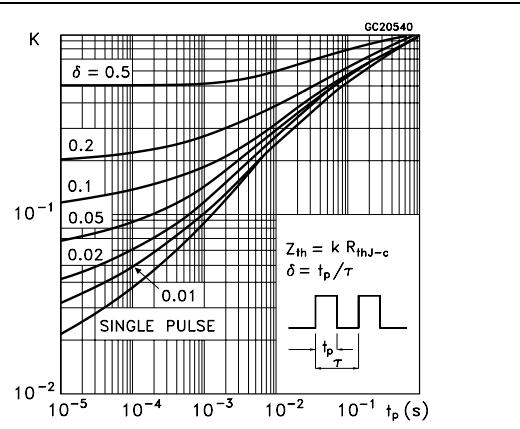


Figure 5. Thermal impedance for TO-247

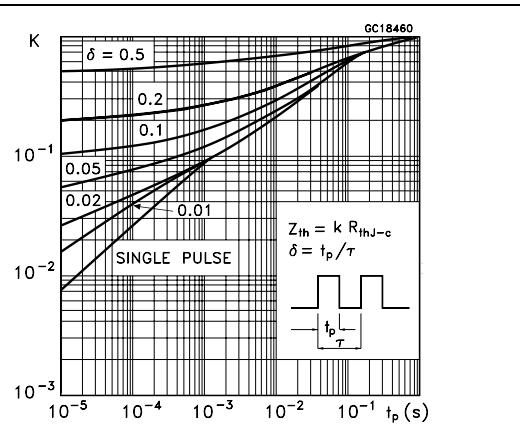


Figure 7. Thermal impedance for TO-220FP

