STP40N20
STB40N20 - STW40N20

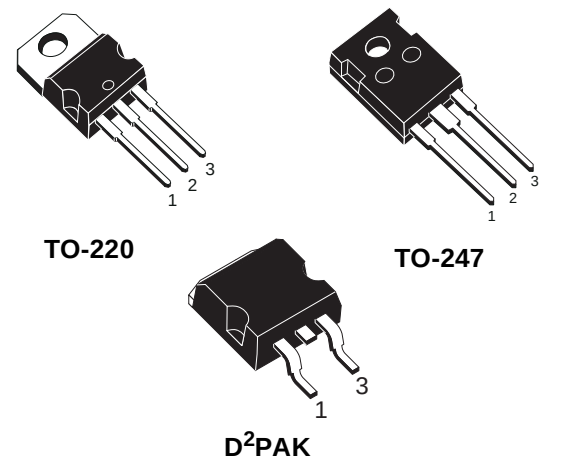
N-CHANNEL 200V - 0.038Ω - 40A TO-220/TO-247/D²PAK
LOW GATE CHARGE STripFET™ MOSFET

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STP40N20	200 V	< 0.045 Ω	40 A	160 W
STW40N20	200 V	< 0.045 Ω	40 A	160 W
STB40N20	200 V	< 0.045 Ω	40 A	160 W

- TYPICAL R_{DS}(on) = 0.038 Ω
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY
- EXCELLENT FIGURE OF MERIT (R_{DS}*Q_g)
- 100% AVALANCHE TESTED

Figure 1: Package



DESCRIPTION

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- UPS

Figure 2: Internal Schematic Diagram

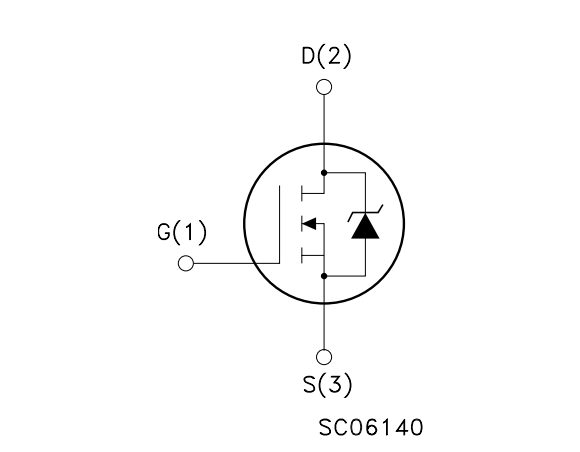


Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP40N20	P40N20	TO-220	TUBE
STW40N20	W40N20	TO-247	TUBE
STB40N20	B40N20	D²PAK	TAPE & REEL

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	200	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	200	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuous) at T_C = 25°C	40	A
I_D	Drain Current (continuous) at T_C = 100°C	25	A
I_{DM} (•)	Drain Current (pulsed)	160	A
P_{TOT}	Total Dissipation at T_C = 25°C	160	W
	Derating Factor	1.28	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	12	V/ns
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150	°C

(●) Pulse width limited by safe operating area
(1) $I_{SD} \leq 40A$, di/dt ≤ 200 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

Table 4: Thermal Data

		TO-220/	TO-247	
Rthj-case	Thermal Resistance Junction-case Max	0.78		°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	50	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300		°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	40	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	230	mJ

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 6: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1mA, V_{GS} = 0	200			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 20 A		0.038	0.045	Ω

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} = 15 V, I_D=20 A		30		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		2500 510 78		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_r	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V_{DD} = 100 V, I_D = 20 A, R_G= 4.7 Ω V_{GS} = 10 V (Resistive Load see, Figure 17)		20 44 74 22		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 160V, I_D = 40 A, V_{GS} = 10V		75 13.2 35.5		nC nC nC

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				40 160	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 20 A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 20 A, di/dt = 100A/µs V_{DD} = 100V, T_j = 25°C (see test circuit, Figure 18)		192 922 9.6		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 20 A, di/dt = 100A/µs V_{DD} = 100V, T_j = 150°C (see test circuit, Figure 18)		242 1440 11.9		ns nC A

(1) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(2) Pulse width limited by safe operating area.

Figure 3: Safe Operating Area For TO-220/ D²PAK

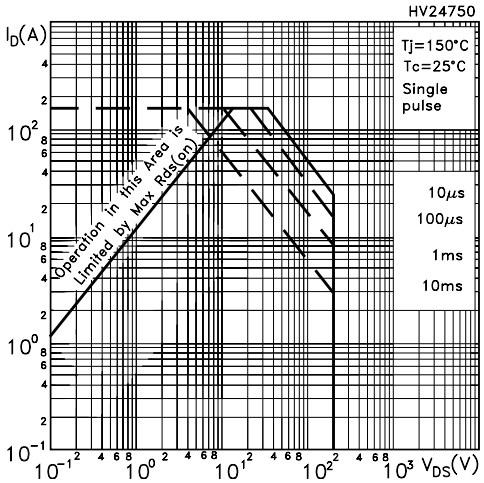


Figure 4: Safe Operating Area For TO-247

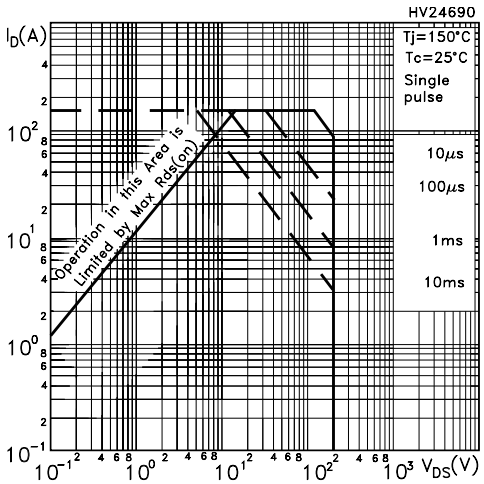


Figure 5: Output Characteristics

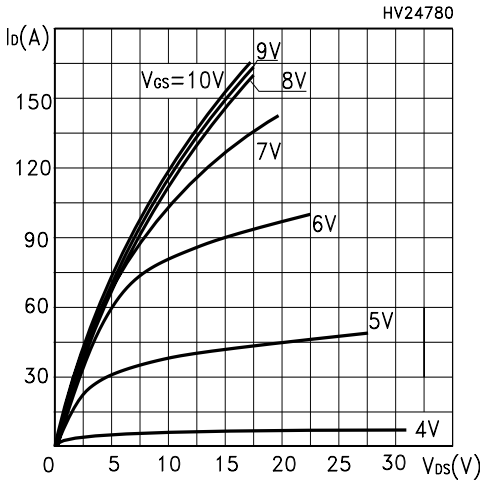


Figure 6: Thermal Impedance For TO-220/ D²PAK

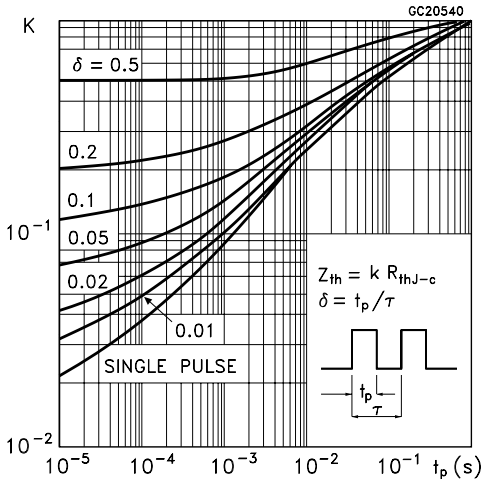


Figure 7: Thermal Impedance For TO-247

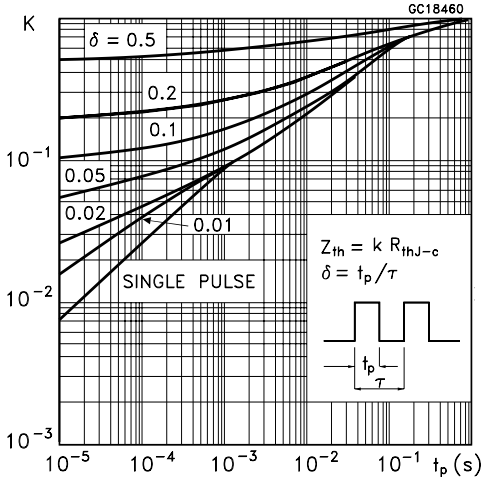


Figure 8: Transfer Characteristics