

STB35N65M5, STF35N65M5, STI35N65M5 STP35N65M5, STW35N65M5

N-channel 650 V, 0.085 Ω 27 A, MDmesh™ V Power MOSFET
in D²PAK, TO-220FP, I²PAK, TO-220, TO-247

Features

Type	V_{DSS} @ T_{JMAX}	$R_{DS(on)}$ max.	I_D
STB35N65M5	710 V	< 0.098 Ω	27 A
STF35N65M5	710 V	< 0.098 Ω	27 A ⁽¹⁾
STI35N65M5	710 V	< 0.098 Ω	27 A
STP35N65M5	710 V	< 0.098 Ω	27 A
STW35N65M5	710 V	< 0.098 Ω	27 A

1. Limited only by maximum temperature allowed

- Worldwide best $R_{DS(on)}$ * area
- Higher V_{DSS} rating
- Excellent switching performance
- Easy to drive
- 100% avalanche tested
- High dv/dt capability

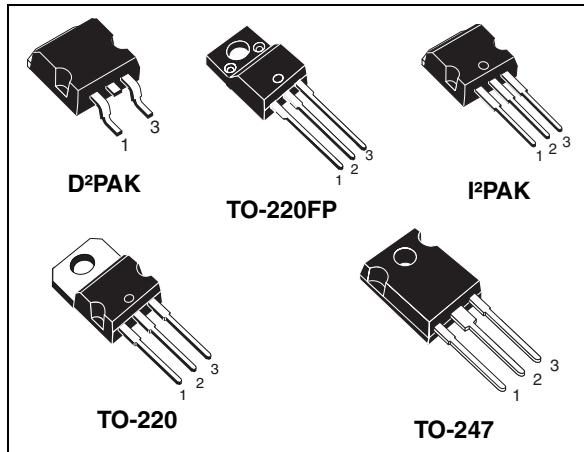
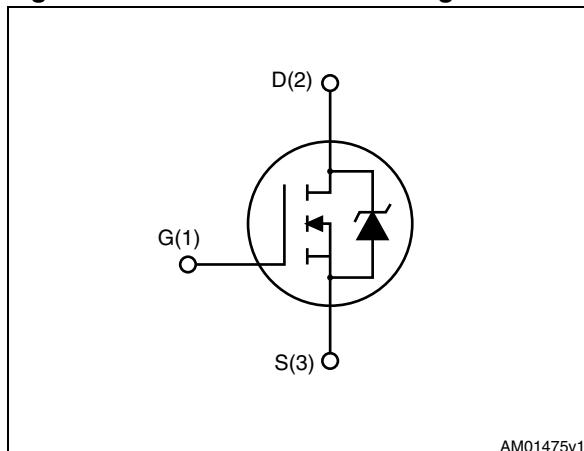


Figure 1. Internal schematic diagram



AM01475v1

Applications

- Switching applications

Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESHTM horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB35N65M5	35N65M5	D ² PAK	Tape and reel
STF35N65M5	35N65M5	TO-220FP	Tube
STI35N65M5	35N65M5	I ² PAK	Tube
STP35N65M5	35N65M5	TO-220	Tube
STW35N65M5	35N65M5	TO-247	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, D ² PAK TO-247, I ² PAK	TO-220FP	
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	27	27 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	17	17 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	108	108 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	160	40	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	9		A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{V}$)	800		mJ
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t=1\text{ s}; T_C=25^\circ\text{C}$)	2500		V
T_{stg}	Storage temperature	- 55 to 150		°C
T_j	Max. operating junction temperature	150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 27\text{ A}$, $dI/dt = 400\text{ A}/\mu\text{s}$, peak $V_{DS} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value					Unit
		D ² PAK	TO-220FP	I ² PAK	TO-220	TO-247	
$R_{thj-case}$	Thermal resistance junction-case max	0.78	3.1	0.78		°C/W	
$R_{thj-amb}$	Thermal resistance junction-ambient max			62.5		50	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max	30					°C/W
T_I	Maximum lead temperature for soldering purpose		300				°C

2 Electrical characteristics

($T_C = 25^\circ\text{C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}, T_C = 125^\circ\text{C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25 \text{ V}$			100	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	3	4	5	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 13.5 \text{ A}$		0.085	0.098	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance					pF
C_{oss}	Output capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz},$ $V_{GS} = 0$	-	3750	-	pF
C_{rss}	Reverse transfer capacitance			84	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0 \text{ to } 520 \text{ V}$	-	220	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related	$V_{GS} = 0, V_{DS} = 0 \text{ to } 520 \text{ V}$	-	75	-	pF
R_G	Intrinsic gate resistance	$f = 1 \text{ MHz open drain}$	-	1.6	-	Ω
Q_g	Total gate charge	$V_{DD} = 520 \text{ V}, I_D = 13.5 \text{ A},$ $V_{GS} = 10 \text{ V}$		83		nC
Q_{gs}	Gate-source charge		-	19	-	nC
Q_{gd}	Gate-drain charge			35		nC

1. $C_{oss\text{ eq}}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. $C_{oss\text{ eq}}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(\text{off})}$	Turn-off delay time	$V_{DD} = 400 \text{ V}, I_D = 16 \text{ A}, R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$	-	60	-	ns
t_r	Rise time			12	-	ns
t_c	Cross time			28	-	ns
t_f	Fall time			16	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		27	A
	Source-drain current (pulsed)				108	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 27 \text{ A}, V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 27 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see)	-	360		ns
	Reverse recovery charge			7		μC
	Reverse recovery current			36		A
t_{rr}	Reverse recovery time	$I_{SD} = 27 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}, T_j = 150^\circ\text{C}$	-	425		ns
	Reverse recovery charge			8		μC
	Reverse recovery current			38		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D²PAK

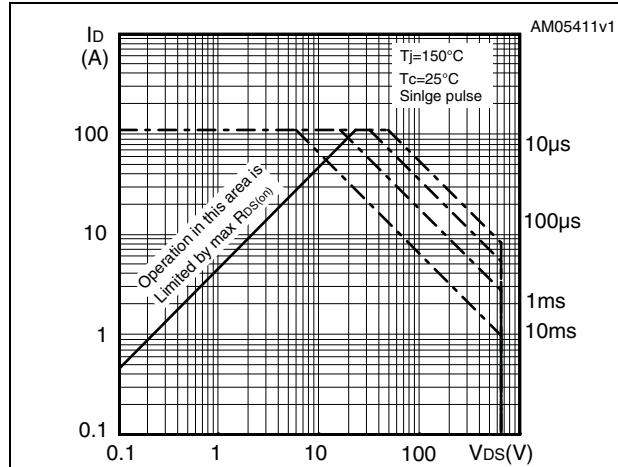


Figure 3. Thermal impedance for TO-220, D²PAK

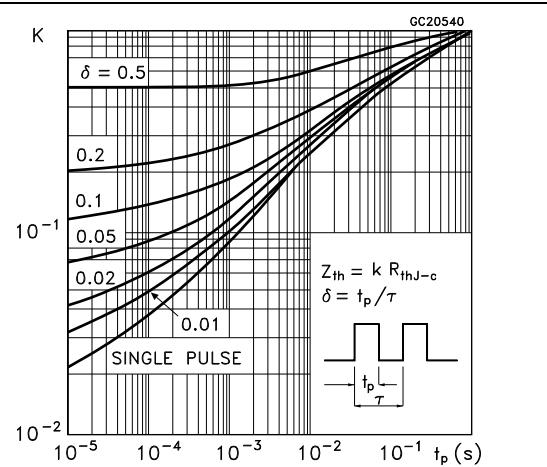


Figure 4. Safe operating area for TO-220FP

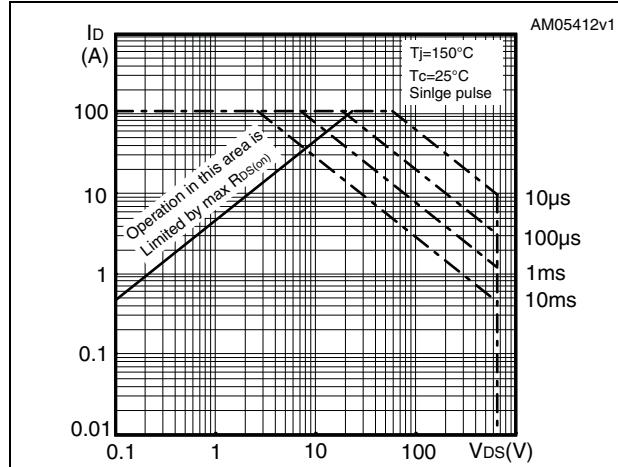


Figure 5. Thermal impedance for TO-220FP

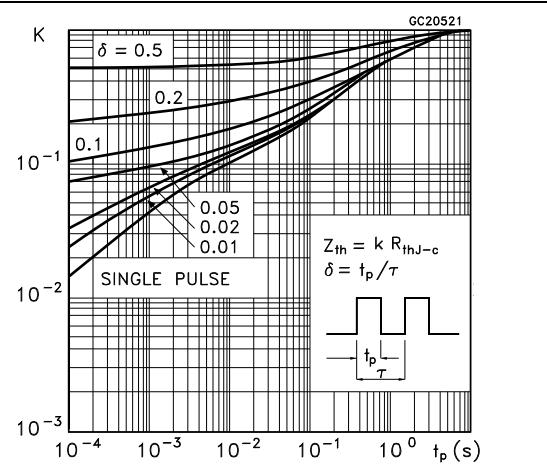


Figure 6. Safe operating area for TO-247

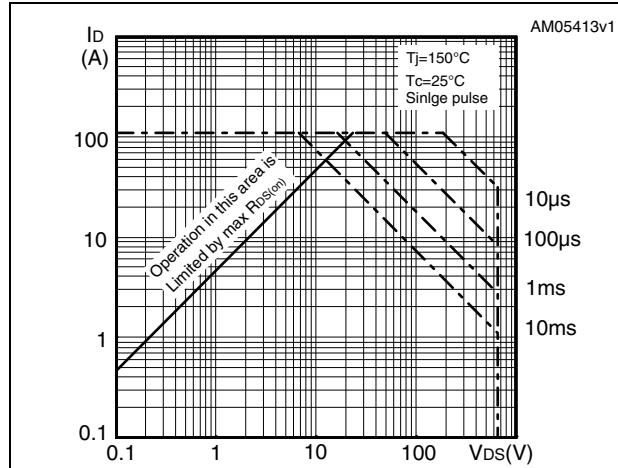


Figure 7. Thermal impedance for TO-247

