STB34N65M5, STI34N65M5, STP34N65M5, STW34N65M5

N-channel 650 V, 0.09 Ω typ., 28 A MDmesh™ V Power MOSFETs in D^2PAK, I^2PAK, TO-220 and TO-247 packages

Datasheet - production data

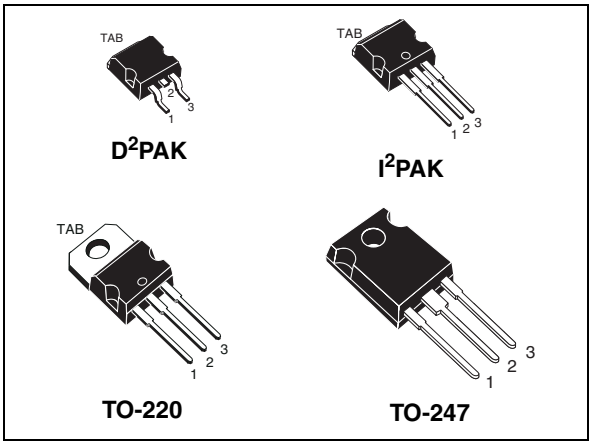
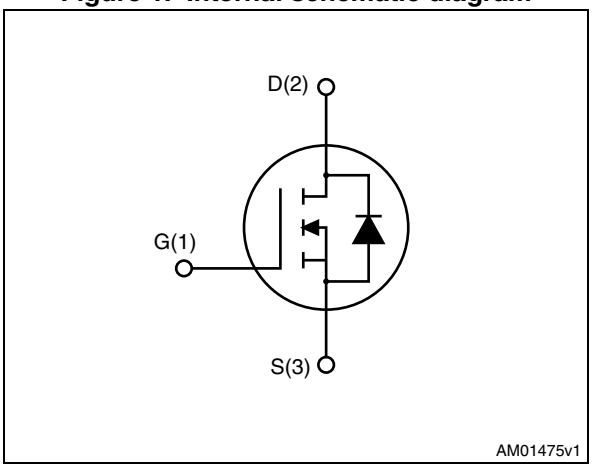


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STB34N65M5	710 V	0.11 Ω	28 A
STI34N65M5			
STP34N65M5			
STW34N65M5			

- Worldwide best $R_{DS(on)}$ * area
- Higher V_{DSS} rating and high dv/dt capability
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STB34N65M5	34N65M5	D^2PAK	Tape and reel
STI34N65M5		I^2PAK	Tube
STP34N65M5		TO-220	
STW34N65M5		TO-247	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	28	A
I_D	Drain current (continuous) at T_C = 100 °C	17.7	A
I_{DM} (1)	Drain current (pulsed)	112	A
P_{TOT}	Total dissipation at T_C = 25 °C	190	W
dv/dt (1)	Peak diode recovery voltage slope	15	V/ns
dv/dt (2)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. $I_{SD} \leq$ 28 A, di/dt $\leq$ 400 A/µs; $V_{DS\ peak} < V_{(BR)DSS}$, V_{DD}=400 V.
2. $V_{DS} \leq$ 480 V

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		D^2PAK	TO-220, I^2PAK	TO-247	
$R_{thj-case}$	Thermal resistance junction-case max	0.66			°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max(1)	30			°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max		62.5	50	°C/W

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	7	A
E_{AS}	Single pulse avalanche energy (starting t_j=25°C, I_d= I_{AR}; V_{dd}=50)	510	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 650 V V_{DS} = 650 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 14 A		0.09	0.11	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	2700	-	pF
C_{oss}	Output capacitance		-	75	-	pF
C_{rss}	Reverse transfer capacitance		-	6.3	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0	-	220	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	63	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	1.95	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 14 A, V_{GS} = 10 V	-	62.5	-	nC
Q_{gs}	Gate-source charge		-	17	-	nC
Q_{gd}	Gate-drain charge		-	28	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_d (v)	Voltage delay time	V_{DD} = 400 V, I_D = 18 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	59	-	ns
t_r (v)	Voltage rise time		-	8.7	-	ns
t_f (i)	Current fall time		-	7.5	-	ns
t_c(off)	Crossing time		-	12	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		28	A
I_{SDM} (1)	Source-drain current (pulsed)		-		112	A
V_{SD} (2)	Forward on voltage	I_{SD} = 28 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 28 A, di/dt = 100 A/µs V_{DD} = 100 V (see	-	350		ns
Q_{rr}	Reverse recovery charge		-	5.6		µC
I_{RRM}	Reverse recovery current		-	32		A
t_{rr}	Reverse recovery time	I_{SD} = 28 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C	-	422		ns
Q_{rr}	Reverse recovery charge		-	7.4		µC
I_{RRM}	Reverse recovery current		-	35		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK, I²PAK and TO-220

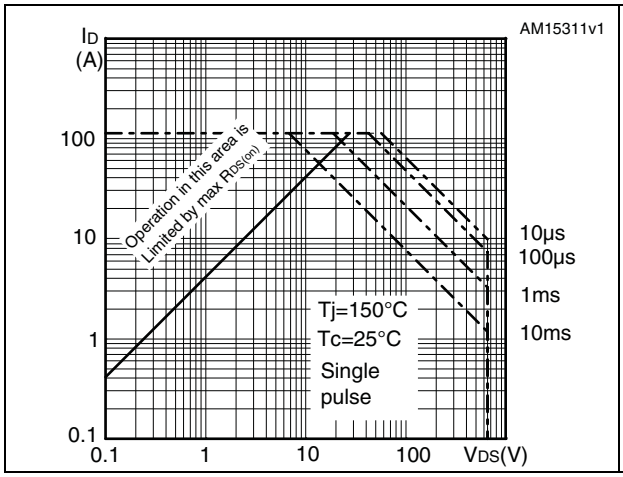


Figure 3. Thermal impedance for D²PAK, I²PAK and TO-220

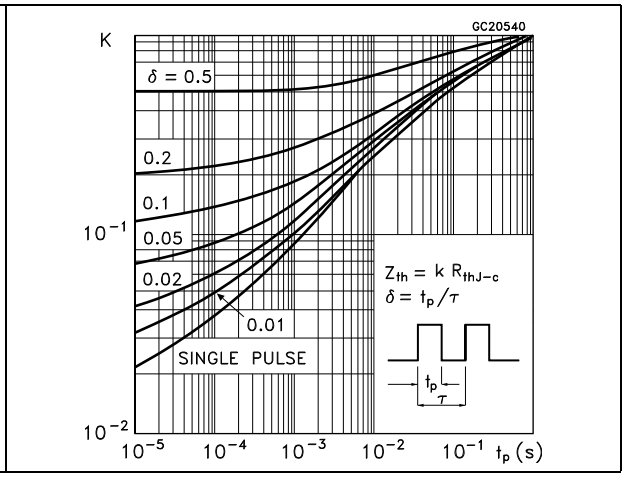


Figure 4. Safe operating area for TO-247

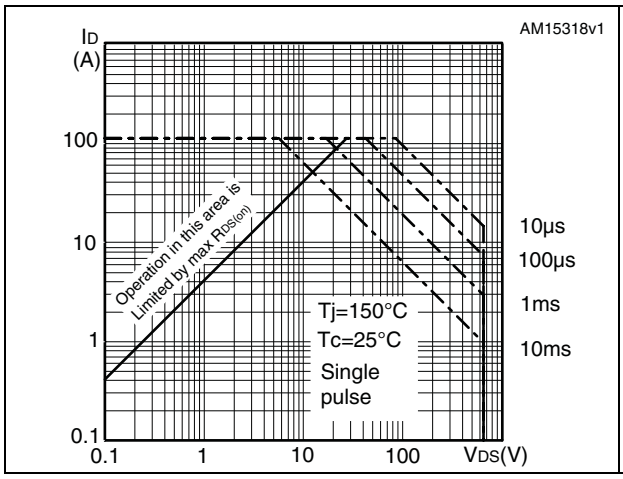


Figure 5. Thermal impedance for TO-247

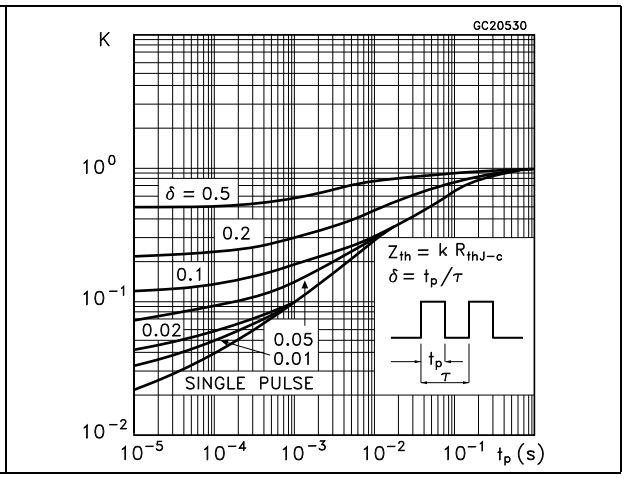


Figure 6. Output characteristics

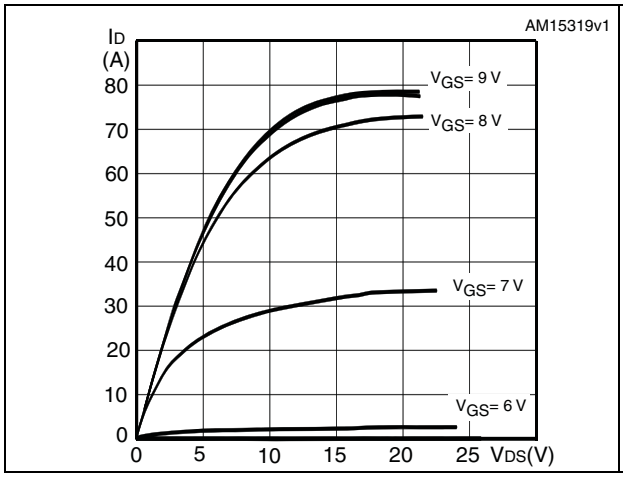


Figure 7. Transfer characteristics