STB32N65M5, STF32N65M5, STI32N65M5 STP32N65M5, STW32N65M5

N-channel 650 V, 0.095 Ω, 24 A, MDmesh™ V Power MOSFET in D²PAK, I²PAK, TO-220FP, TO-220, TO-247

Features

Order codes	V_{DSS}@ T_{Jmax}	$R_{DS(on)}$ max	I_D
STB32N65M5	710 V	< 0.119 Ω	24 A
STF32N65M5	710 V	< 0.119 Ω	24 A(1)
STI32N65M5	710 V	< 0.119 Ω	24 A
STP32N65M5	710 V	< 0.119 Ω	24 A
STW32N65M5	710 V	< 0.119 Ω	24 A

1. Limited only by maximum temperature allowed

- Worldwide best $R_{DS(on)}$* area
- Higher V_{DSS} rating
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

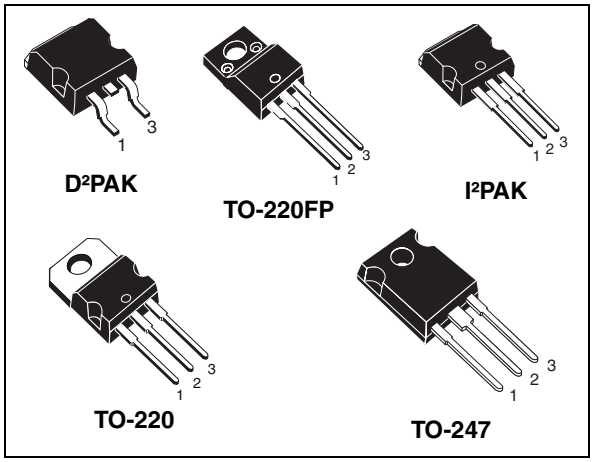
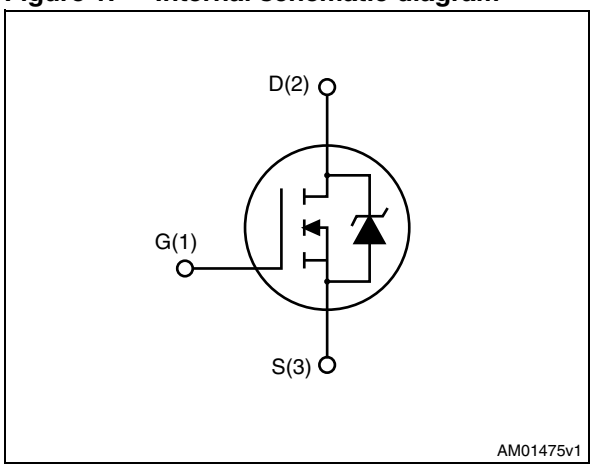


Figure 1. Internal schematic diagram



Applications

- Switching applications

Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB32N65M5	32N65M5	D²PAK	Tape and reel
STF32N65M5	32N65M5	TO-220FP	Tube
STI32N65M5	32N65M5	I²PAK	Tube
STP32N65M5	32N65M5	TO-220	Tube
STW32N65M5	32N65M5	TO-247	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, D²PAK TO-247, I²PAK	TO-220FP	
V_{GS}	Gate- source voltage	± 25		V
I_D	Drain current (continuous) at T_C = 25 °C	24	24(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	15	15 (1)	A
I_{DM} (2)	Drain current (pulsed)	96	96 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	150	35	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	8		A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	650		mJ
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)		2500	V
T_{stg}	Storage temperature	- 55 to 150		°C
T_j	Max. operating junction temperature	150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 24$ A, di/dt = 400 A/µs, peak $V_{DS} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value					Unit
		D²PAK	TO-220FP	I²PAK	TO-220	TO-247	
$R_{thj-case}$	Thermal resistance junction-case max	0.83	3.6	0.83			°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max		62.5			50	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max	30					°C/W
T_l	Maximum lead temperature for soldering purpose		300				°C

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 12 A		0.095	0.119	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	3320 75 5	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 520 V	-	210	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related	V_{GS} = 0, V_{DS} = 0 to 520 V	-	70	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	2	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 12 A, V_{GS} = 10 V	-	72 17 29	-	nC nC nC

1. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. $C_{oss\ eq.}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_r t_c t_f	Turn-off delay time Rise time Cross time Fall time	V_{DD} = 400 V, I_D = 15 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	53 12 29 16	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		24 96	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 24 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 24 A, di/dt = 100 A/µs V_{DD} = 60 V (see)	-	375 6 33		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 24 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C	-	440 8 36		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D²PAK, I²PAK

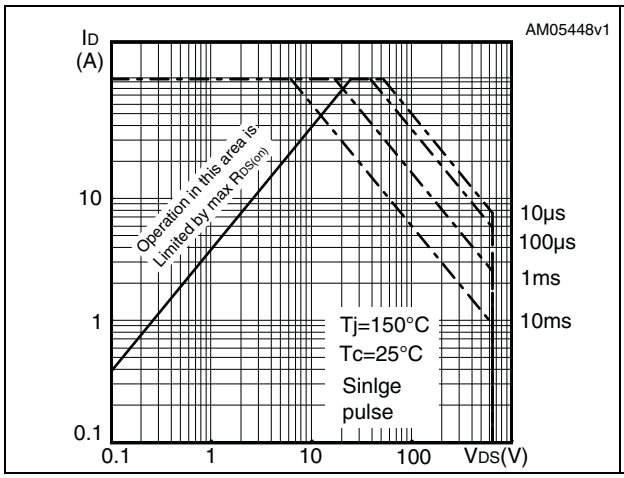


Figure 3. Thermal impedance for TO-220, D²PAK, I²PAK

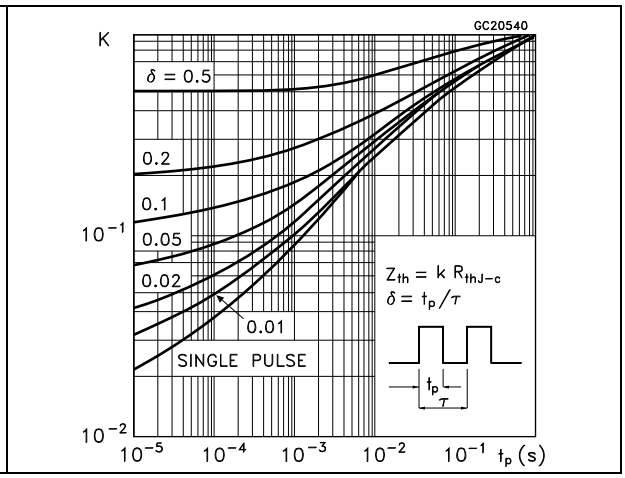


Figure 4. Safe operating area for TO-220FP

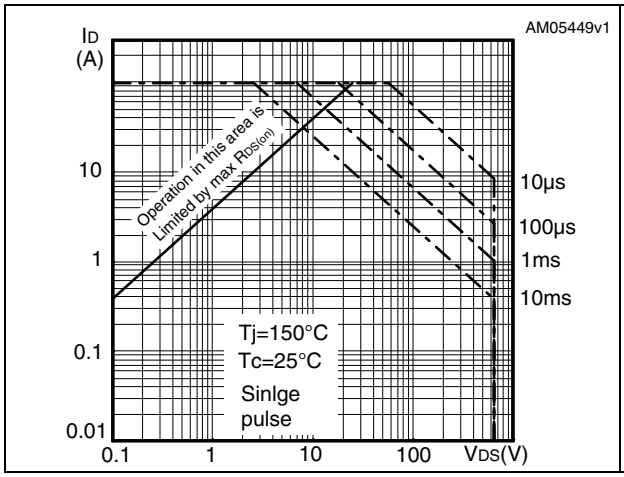


Figure 5. Thermal impedance for TO-220FP

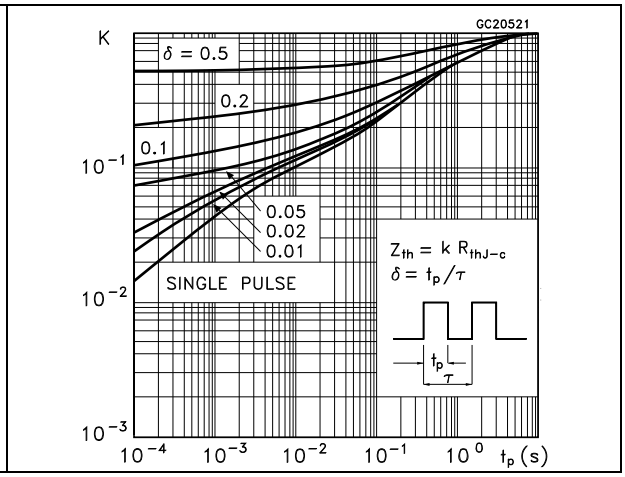


Figure 6. Safe operating area for TO-247

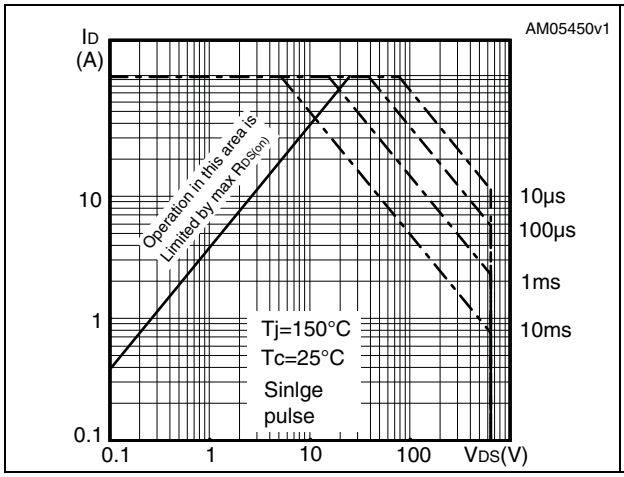


Figure 7. Thermal impedance for TO-247