STB28N65M2, STF28N65M2, STP28N65M2, STW28N65M2

N-channel 650 V, 0.15 Ω typ., 20 A MDmesh™ M2 Power MOSFETs in D²PAK, TO-220FP, TO-220 and TO-247 packages

Datasheet - preliminary data

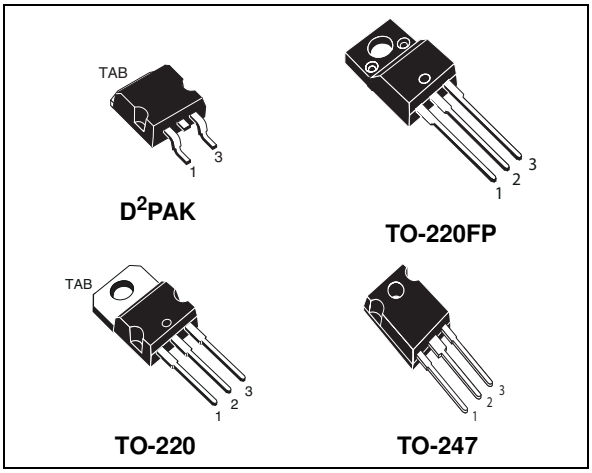
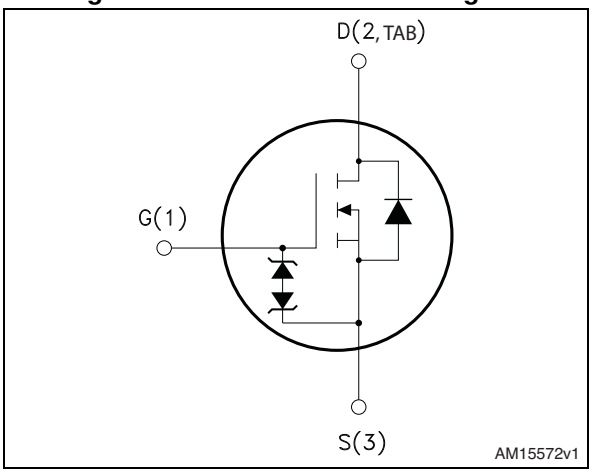


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max	I_D
STB28N65M2	650 V	0.18 Ω	20 A
STF28N65M2			
STP28N65M2			
STW28N65M2			

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, the devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB28N65M2	28N65M2	D²PAK	Tape and reel
STF28N65M2		TO-220FP	Tube
STP28N65M2		TO-220	
STW28N65M2		TO-247	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D^2PAK, TO-220, TO-247	TO-220FP	
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at T_C = 25 °C	20	20(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	13	13(1)	A
I_{DM} (2)	Drain current (pulsed)	80		A
P_{TOT}	Total dissipation at T_C = 25 °C	170	30	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)		2500	V
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50		
T_{stg}	Storage temperature	- 55 to 150		°C
T_j	Max. operating junction temperature	150		

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 20$ A, di/dt ≤ 400 A/µs; $V_{DS\ peak} < V_{(BR)DSS}$, V_{DD}=520 V
4. $V_{DS} \leq 520$ V

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		D^2PAK	TO-220FP	TO-220	TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.74	4.17	0.74		°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb max	30				°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max		62.5		50	°C/W

1. When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	2.4	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, $I_D = I_{AR}$; V_{DD} = 50 V)	760	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 650 V			1	µA
		V_{GS} = 0, V_{DS} = 650 V T_C = 125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10 A		0.15	0.18	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	1440	-	pF
C_{oss}	Output capacitance		-	60	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\ eq}$(1)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 520 V	-	307	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	4.9	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 20 A, V_{GS} = 10 V	-	35	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	15	-	nC

1. Coss eq. is defined as a constant equivalent capacitance giving the same charging time as Coss when VDS increases from 0 to 80% VDSS

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 10 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	13.4	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time		-	59	-	ns
t_f	Fall time		-	8.8	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		20	A
I_{SDM} (1)	Source-drain current (pulsed)		-		80	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0, I_{SD} = 20 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs V_{DD} = 60 V (see	-	384		ns
Q_{rr}	Reverse recovery charge		-	5.7		µC
I_{RRM}	Reverse recovery current		-	30		A
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs V = 60 V, T = 150 °C	-	544		ns
Q_{rr}	Reverse recovery charge		-	8.2		µC
I_{RRM}	Reverse recovery current		-	30.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK and TO-220

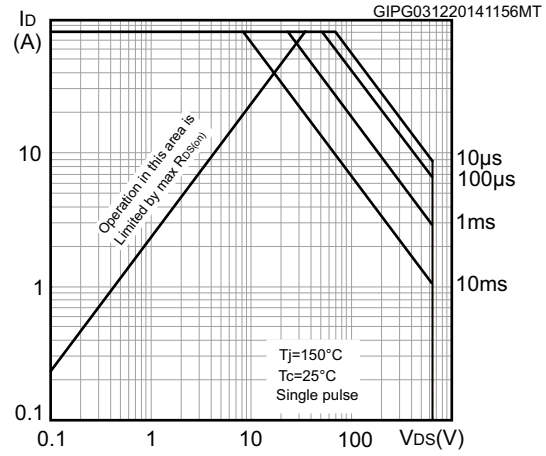


Figure 3. Thermal impedance for D²PAK and TO-220

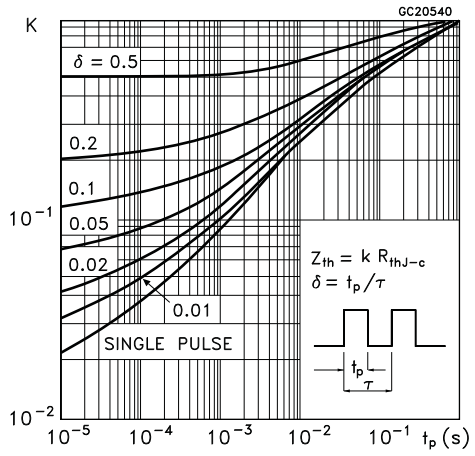


Figure 4. Safe operating area for TO-220FP

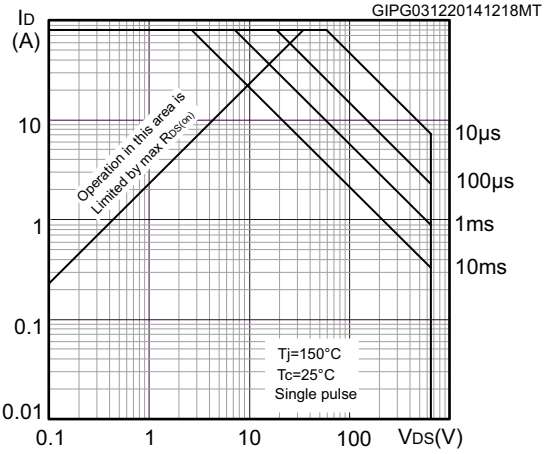


Figure 5. Thermal impedance for TO-220FP

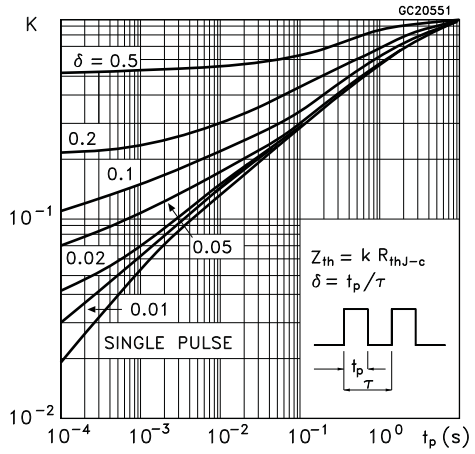


Figure 6. Safe operating area for TO-247

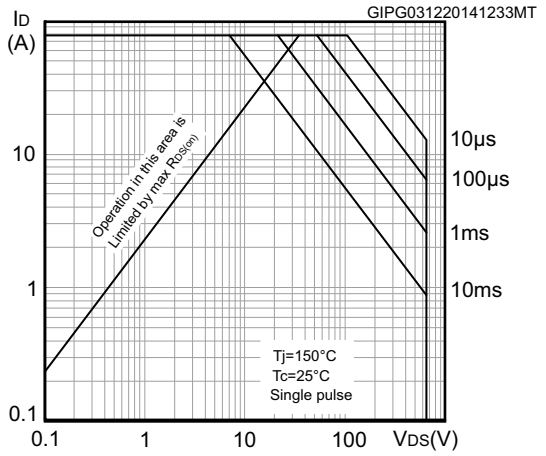


Figure 7. Thermal impedance for TO-247