

STB28N60M2, STI28N60M2, STP28N60M2, STW28N60M2

N-channel 600 V, 0.135 Ω typ., 22 A MDmesh™ M2
Power MOSFETs in D²PAK, I²PAK, TO-220 and TO-247

Datasheet - production data

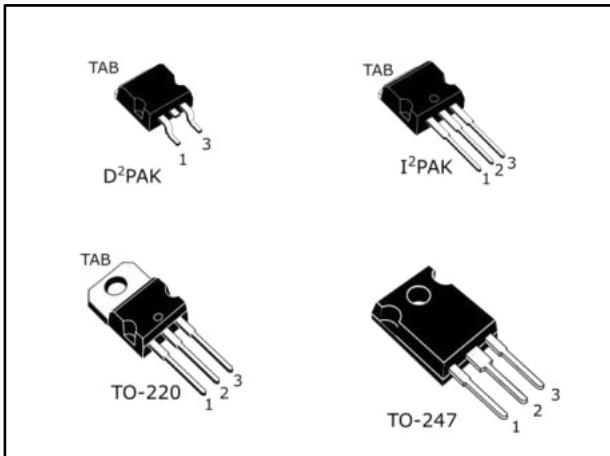
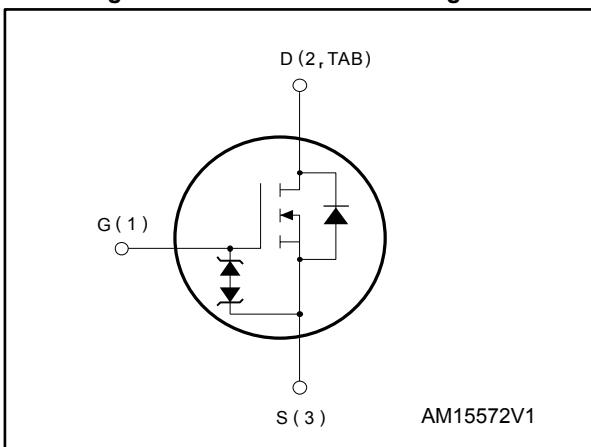


Figure 1: Internal schematic diagram



Features

Order code	V _{DS} @ T _{Jmax}	R _{D(on)} max.	I _D
STB28N60M2			
STI28N60M2	650 V	0.150 Ω	
STP28N60M2			22 A
STW28N60M2			

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LCC converters, resonant converters

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STB28N60M2	28N60M2	D ² PAK	Tape and reel
STI28N60M2		I ² PAK	
STP28N60M2		TO-220	
STW28N60M2		TO-247	Tube

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	22	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	14	A
$I_{DM}^{(1)}$	Drain current (pulsed)	88	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	170	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

Notes:

(¹)Pulse width limited by safe operating area.

(²) $I_{SD} \leq 22$ A, $di/dt \leq 400$ A/ μs ; $V_{DS(\text{peak})} < V_{(\text{BR})DSS}$, $V_{DD} = 400$ V.

(³) $V_{DS} \leq 480$ V

Table 3: Thermal data

Symbol	Parameter	Value				Unit
		D ² PAK	I ² PAK	TO-220	TO-247	
$R_{thj-case}$	Thermal resistance junction-case max	0.74		$^\circ\text{C/W}$		$^\circ\text{C/W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max ⁽¹⁾	30				$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max		62.5	62.5	50	$^\circ\text{C/W}$

Notes:

(¹)When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{j\max}$)	3.6	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$; $V_{DD} = 50$ V)	350	mJ

2 Electrical characteristics

$T_C = 25^\circ\text{C}$ unless otherwise specified.

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}$			1	μA
		$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}, T_C = 125^\circ\text{C}$ ⁽¹⁾			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			± 10	μA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2	3	4	V
$R_{DS(\text{on})}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 11 \text{ A}$		0.135	0.150	Ω

Notes:

(1) Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0 \text{ V}$	-	1440	-	pF
C_{oss}	Output capacitance		-	70	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss \text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0 \text{ to } 480 \text{ V}, V_{GS} = 0 \text{ V}$	-	104	-	pF
R_G	Intrinsic gate resistance	$f = 1 \text{ MHz}$ open drain	-	5.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 480 \text{ V}, I_D = 22 \text{ A}, V_{GS} = 0 \text{ to } 10 \text{ V}$ (see)	-	36	-	nC
Q_{gs}	Gate-source charge		-	7.2	-	nC
Q_{gd}	Gate-drain charge		-	16	-	nC

Notes:

(1) $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80 % V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300 \text{ V}, I_D = 11 \text{ A}, R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$	-	14.5	-	ns
t_r	Rise time		-	7.2	-	ns
$t_{d(off)}$	Turn-off-delay time		-	100	-	ns
t_f	Fall time		-	8	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		22	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		88	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$, $I_{SD} = 22 \text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 22 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$ (see)	-	350		ns
Q_{rr}	Reverse recovery charge		-	4.7		μC
I_{RRM}	Reverse recovery current		-	27		A
t_{rr}	Reverse recovery time	$I_{SD} = 22 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$	-	451		ns
Q_{rr}	Reverse recovery charge		-	6.5		μC
I_{RRM}	Reverse recovery current		-	29		A

Notes:

⁽¹⁾Pulse width is limited by safe operating area.

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5 %.

Electrical characteristics

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2.1 Electrical characteristics (curves)

