# STB24N60DM2, STP24N60DM2, STW24N60DM2

## N-channel 600 V, 0.175 Ω typ., 18 A FDmesh II Plus™ low $Q_g$ Power MOSFETs in $D^2$PAK, TO-220 and TO-247 packages

**Datasheet — production data**

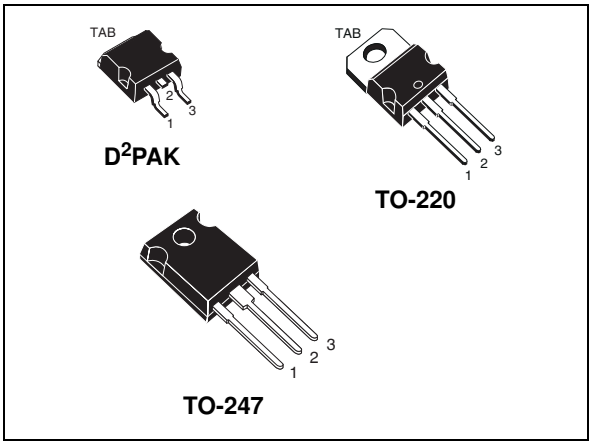
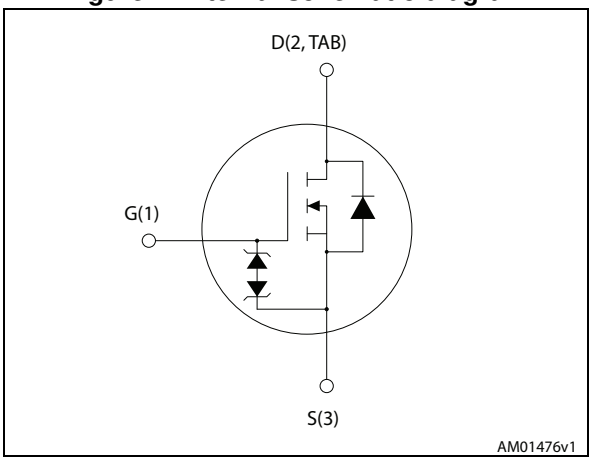



**Figure 1. Internal schematic diagram**




## Features

| Order codes | $V_{DS}$ @ $T_{Jmax}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STB24N60DM2 | 650 V | 0.20 Ω | 18 A |
| STP24N60DM2 | | | |
| STW24N60DM2 | | | |

- Extremely low gate charge and input capacitance
- Lower $R_{DS(on)}$ x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected
- Extremely high dv/dt and avalanche capabilities

## Applications

- Switching applications

## Description

These FDmesh II Plus™ low $Q_g$ Power MOSFETs with intrinsic fast-recovery body diode are produced using a new generation of MDmesh™ technology: MDmesh II Plus™ low $Q_g$. These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

**Table 1. Device summary**

| Order codes | Marking | Package | Packaging |
|---|---|---|---|
| STB24N60DM2 | 24N60DM2 | $D^2$PAK | Tape and reel |
| STP24N60DM2 | | TO-220 | Tube |
| STW24N60DM2 | | TO-247 | |

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ± 25 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 18 | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 11 | A |
| $I_{DM}$ (1) | Drain current (pulsed) | 72 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 150 | W |
| dv/dt (2) | Peak diode recovery voltage slope | 40 | V/ns |
| dv/dt(3) | MOSFET dv/dt ruggedness | 50 | V/ns |
| $T_{stg}$ | Storage temperature | - 55 to 150 | °C |
| $T_j$ | Max. operating junction temperature | | |

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 18$ A, di/dt $\leq 400$ A/$\mu$s; $V_{DS\ peak} < V_{(BR)DSS}$, $V_{DD}$=400 V.
3. $V_{DS} \leq 480$ V

**Table 3. Thermal data**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | $D^2PAK$ | TO-220 | TO-247 | |
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 0.83 | | | °C/W |
| $R_{thj\text{-}pcb}$ | Thermal resistance junction-pcb max(1) | 30 | | | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient max | | 62.5 | 50 | °C/W |

1. When mounted on 1 inch² FR-4, 2 Oz copper board

**Table 4. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ ) | 3.5 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j$=25°C, $I_D$= $I_{AR}$; $V_{DD}$=50) | 180 | mJ |

# 2 Electrical characteristics

($T_C$ = 25 °C unless otherwise specified)

**Table 5. On /off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 | 600 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = 600 V | | | 1.5 | µA |
| | | $V_{DS}$ = 600 V, $T_C$=125 °C | | | 100 | µA |
| $I_{GSS}$ | Gate-body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ± 25 V | | | ±10 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 9 A | | 0.175 | 0.200 | Ω |

**Table 6. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 | - | 1055 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 56 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 2.4 | - | pF |
| $C_{oss\ eq.}$ (1) | Equivalent output capacitance | $V_{DS}$ = 0 to 480 V, $V_{GS}$ = 0 | - | 259 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz, $I_D$ = 0 | - | 7 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 480 V, $I_D$ = 18 A, $V_{GS}$ = 10 V | - | 29 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 6 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 12 | - | nC |

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

**Table 7. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 300 V, $I_D$ = 9 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V | - | 15 | - | ns |
| $t_r$ | Rise time | | - | 8.7 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 60 | - | ns |
| $t_f$ | Fall time | | - | 15 | - | ns |

**Table 8. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$(1) | Source-drain current | | - | | 18 | A |
| $I_{SDM}$ (2) | Source-drain current (pulsed) | | - | | 72 | A |
| $V_{SD}$(3) | Forward on voltage | $I_{SD}$ = 18 A, $V_{GS}$ = 0 | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 18 A, di/dt = 100 A/$\mu$s $V_{DD}$ = 60 V (see | - | 155 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 956 | | nC |
| $I_{RRM}$ | Reverse recovery current | | - | 12.5 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 18 A, di/dt = 100 A/$\mu$s $V_{DD}$ = 60 V, $T_j$ = 150 °C | - | 200 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 1450 | | nC |
| $I_{RRM}$ | Reverse recovery current | | - | 13 | | A |

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area.
3. Pulsed: pulse duration = 300 $\mu$s, duty cycle 1.5%