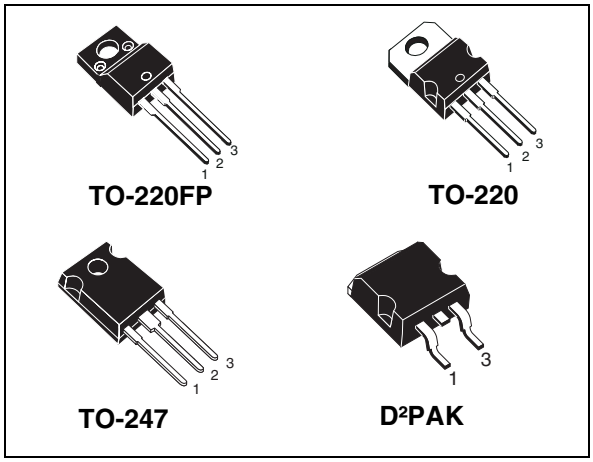
STB23NM50N, STF23NM50N STP23NM50N, STW23NM50N

N-channel 500 V, 0.162 Ω, 17 A TO-220, TO-220FP, TO-247, D²PAK
MDmesh™ II Power MOSFET

Features

Order codes	V_{DSS} (@Tjmax)	$R_{DS(on)}$ max.	I_D
STB23NM50N	550 V	< 0.19 Ω	17 A
STF23NM50N			
STP23NM50N			
STW23NM50N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Application

Switching applications

Description

These devices are made using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

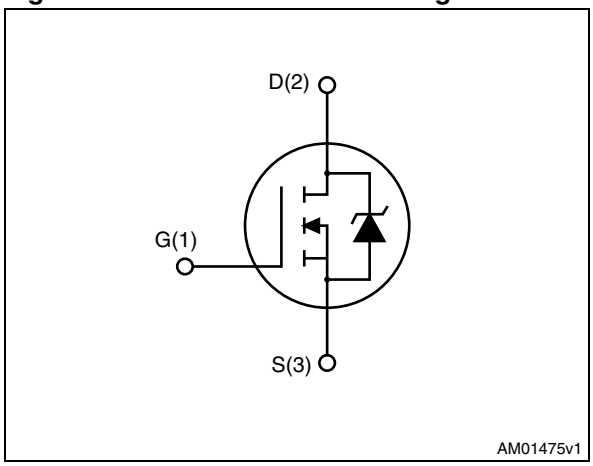


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB23NM50N	23NM50N	D²PAK	Tape and reel
STF23NM50N		TO-220FP	Tube
STP23NM50N		TO-220	
STW23NM50N		TO-247	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		TO-220, D²PAK	TO-247	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	500			V
V_{GS}	Gate- source voltage	± 25			V
I_D	Drain current (continuous) at T_C = 25 °C	17		17 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	11		11 (1)	A
I_{DM} (2)	Drain current (pulsed)	68		68 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	125		30	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)			2500	V
dv/dt (3)	Peak diode recovery voltage slope	15			V/ns
T_{stg}	Storage temperature	-55 to 150			°C
T_j	Max. operating junction temperature	150			°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq$ 17 A, di/dt $\leq$ 400 A/µs, V_{DS} peak $\leq$ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		D²PAK	TO-247	TO-220	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	1			4.17	°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-pcb minimum footprint	30				°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max		62.5	50	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose		300			°C

1. When mounted on 1inch² FR-4 board, 2 oz Cu

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	6	A
E_{AS}	Single pulse avalanche energy (starting Tj = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	254	mJ

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating, @125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 8.5 A		0.162	0.19	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	1330 84 4.8	-	pF pF pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 400 V	-	210	-	pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 400 V, I_D = 17 A, V_{GS} = 10 V,	-	45 7 24	-	nC nC nC
R_g	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level=20 mV open drain	-	4.6	-	Ω

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V, I_D = 17 A R_G = 4.7 Ω V_{GS} = 10 V	-	6.6	-	ns
t_r	Rise time			19		ns
$t_{d(off)}$	Turn-off-delay time			71		ns
t_f	Fall time			29		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		17	A
I_{SDM} (1)	Source-drain current (pulsed)				68	A
V_{SD} (2)	Forward on voltage	I_{SD} = 17 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 17 A, di/dt = 100 A/µs V_{DD} = 60 V	-	286		ns
Q_{rr}	Reverse recovery charge			3700		nC
I_{RRM}	Reverse recovery current			26		A
t_{rr}	Reverse recovery time	I_{SD} = 17 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C	-	350		ns
Q_{rr}	Reverse recovery charge			4800		nC
I_{RRM}	Reverse recovery current			27		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D²PAK

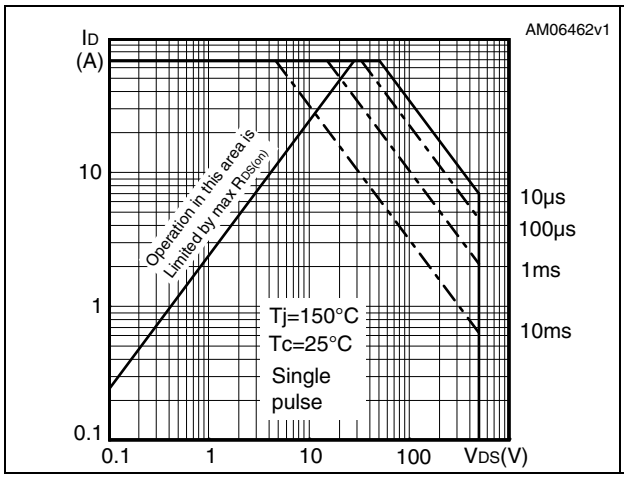


Figure 3. Thermal impedance for TO-220, D²PAK

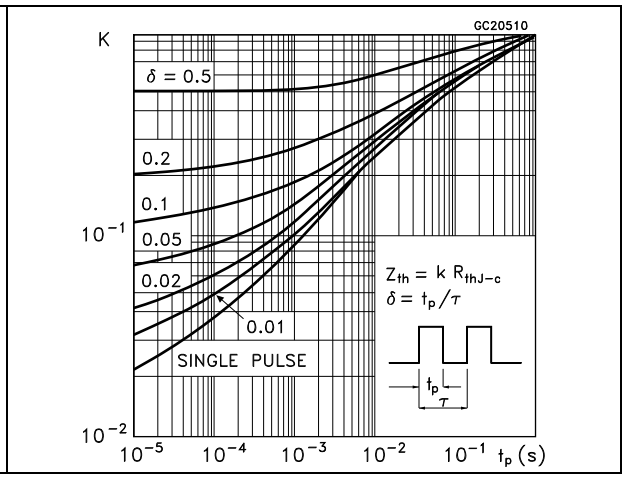


Figure 4. Safe operating area for TO-220FP

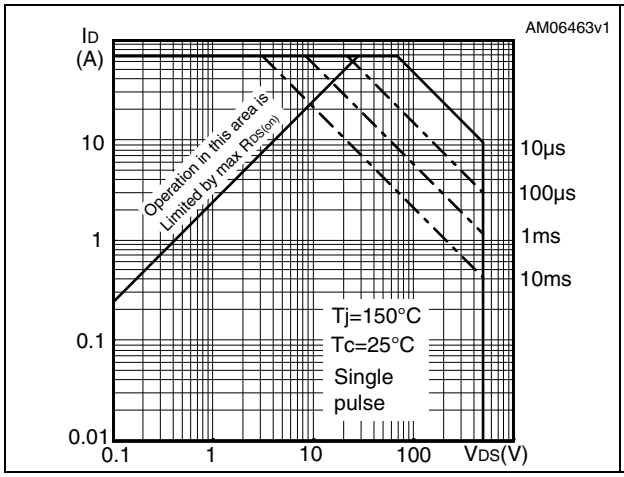


Figure 5. Thermal impedance for TO-220FP

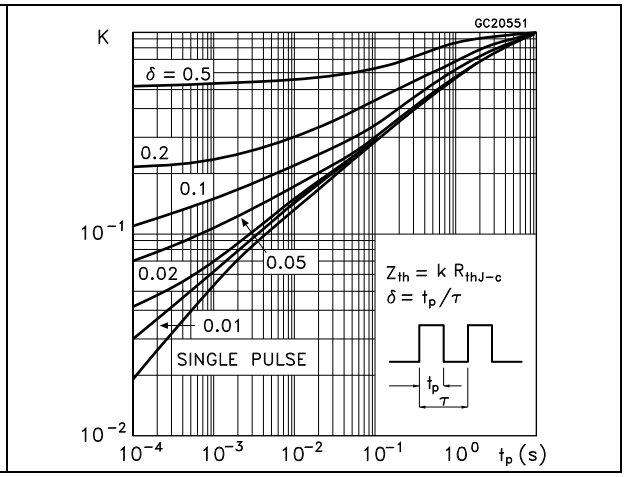


Figure 6. Safe operating area for TO-247

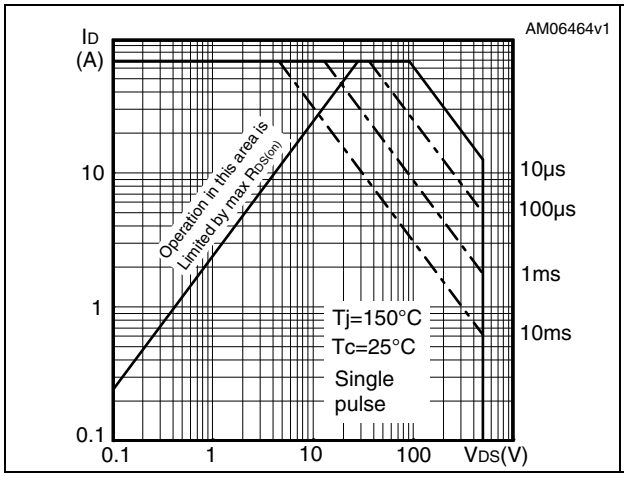


Figure 7. Thermal impedance for TO-247