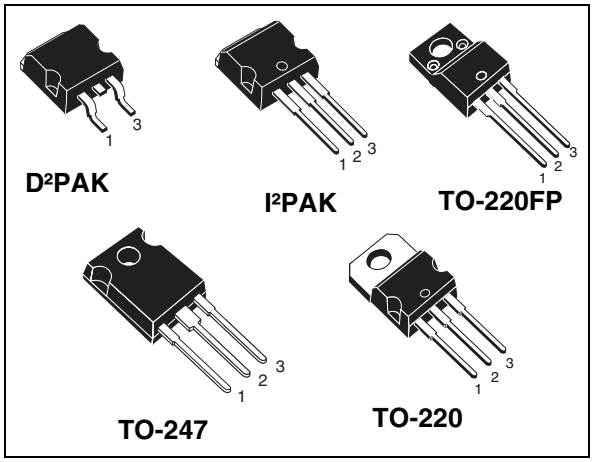
STB22NM60N, STF22NM60N, STI22NM60N STP22NM60N, STW22NM60N

N-channel 600 V, 0.2 Ω, 16 A MDmesh™ II Power MOSFET in D^2PAK, TO-220FP, I^2PAK, TO-220 and TO-247

Features

Order codes	V_{DSS} (@Tjmax)	$R_{DS(on)}$ max.	I_D
STB22NM60N	650 V	< 0.22 Ω	16 A
STF22NM60N	650 V	< 0.22 Ω	16 A
STI22NM60N	650 V	< 0.22 Ω	16 A
STP22NM60N	650 V	< 0.22 Ω	16 A
STW22NM60N	650 V	< 0.22 Ω	16 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Application

Switching applications

Description

These devices are made using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

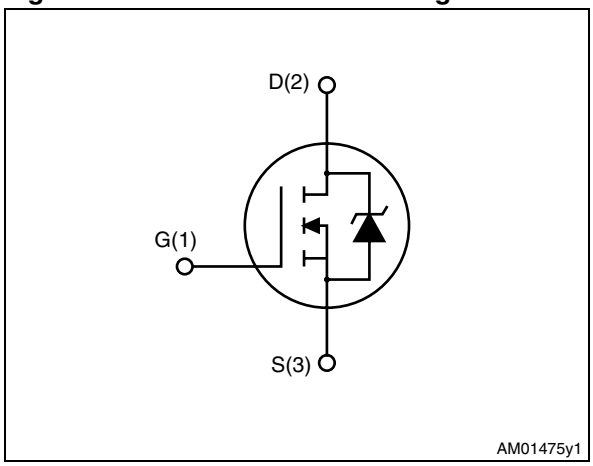


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB22NM60N	22NM60N	D²PAK	Tape and reel
STF22NM60N		TO-220FP	Tube
STI22NM60N		I²PAK	
STP22NM60N		TO-220	
STW22NM60N		TO-247	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		D²PAK I²PAK	TO-220 TO-247	TO-220FP	
V_{GS}	Gate- source voltage	± 30			V
I_D	Drain current (continuous) at T_C = 25 °C	16		16 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	10		10 (1)	A
I_{DM} (2)	Drain current (pulsed)	64		64 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	125		30	W
dv/dt(3)	Peak diode recovery voltage slope	15			V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)			2500	V
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150			°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 16$ A, di/dt $\leq$ 400 A/µs, $V_{DSpeak} \leq V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value					Unit
		D²PAK	I²PAK	TO-220	TO-247	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max.	1				4.17	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max.		62.5		50	62.5	°C/W
$R_{thj-pcb}$(1)	Thermal resistance junction-pcb max.	30					°C/W
T_J	Maximum lead temperature for soldering purpose		300				°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu

Table 4. Thermal data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	6	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	300	mJ

2 Electrical characteristics

(Tcase = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 8 A		0.2	0.22	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	1330 84 4.6	-	pF pF pF
$C_{oss\ eq.}$ (1)	Output equivalent capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0	-	181	-	pF
R_g	Gate input resistance	f=1 MHz open drain	-	4.7	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 480 V, I_D = 16 A, V_{GS} = 10 V	-	44 6 25	-	nC nC nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}.

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 8 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	11	-	ns
$t_{r(v)}$	Voltage rise time			18		ns
$t_{d(off)}$	Turn-off delay time			74		ns
$t_{f(i)}$	Fall time			38		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		16	A
I_{SDM} (1)	Source-drain current (pulsed)				64	A
V_{SD} (2)	Forward on voltage	I_{SD} = 16 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 16 A, di/dt = 100 A/µs V_{DD}= 60 V	-	296		ns
Q_{rr}	Reverse recovery charge			4		µC
I_{RRM}	Reverse recovery current			26.8		A
t_{rr}	Reverse recovery time	I_{SD} = 16 A, di/dt = 100 A/µs V_{DD}= 60 V T_J = 150 °C	-	350		ns
Q_{rr}	Reverse recovery charge			4.7		µC
I_{RRM}	Reverse recovery current			27		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D²PAK, I²PAK

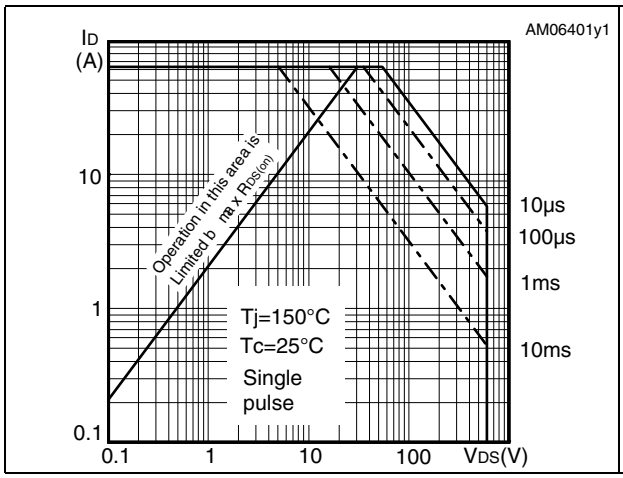


Figure 3. Thermal impedance for TO-220, D²PAK, I²PAK

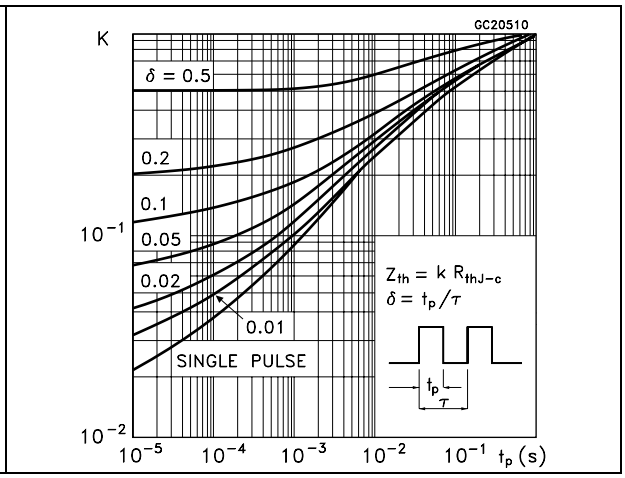


Figure 4. Safe operating area for TO-220FP

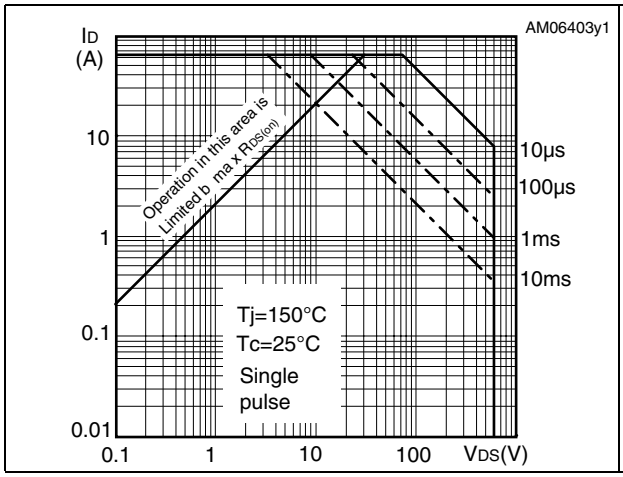


Figure 5. Thermal impedance for TO-220FP

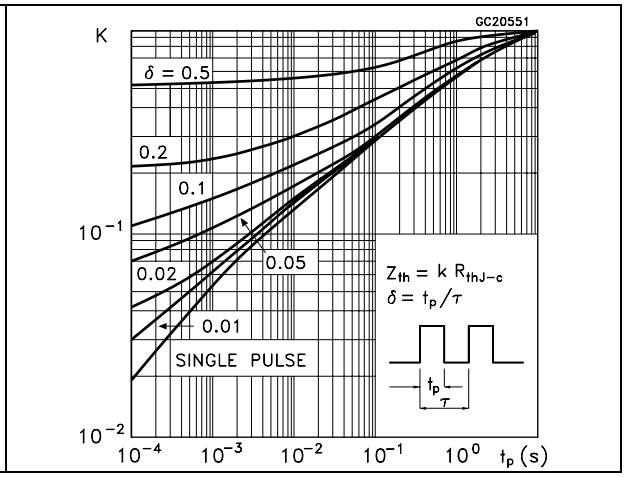


Figure 6. Safe operating area for TO-247

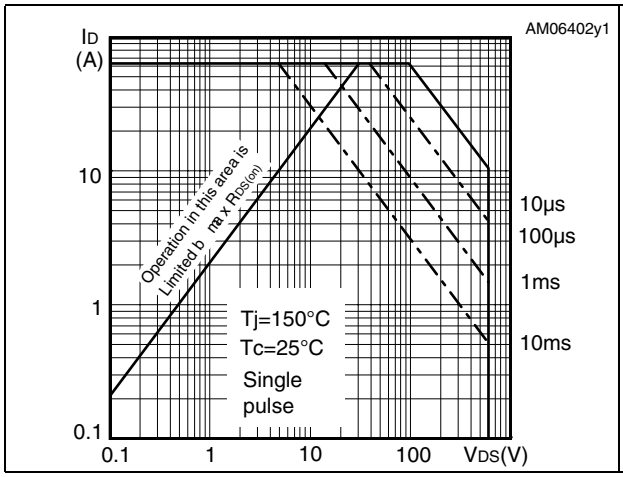


Figure 7. Thermal impedance for TO-247