STP/F21NM50N - STW21NM50N
STB21NM50N - STB21NM50N-1

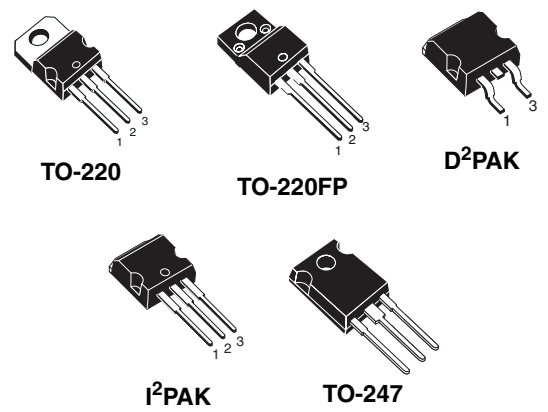
N-channel 500V - 0.15Ω - 18A TO-220/FP/D^2/I^2PAK/TO-247
Second generation MDmesh™ Power MOSFET

General features

Type	V_{DSS} (@Tjmax)	$R_{DS(on)}$	I_D
STB21NM50N	550V	< 0.19Ω	18A
STB21NM50N-1	550V	< 0.19Ω	18A
STF21NM50N	550V	< 0.19Ω	18A(1)
STP21NM50N	550V	< 0.19Ω	18A
STW21NM50N	550V	< 0.19Ω	18A

1. Limited by wire bonding

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



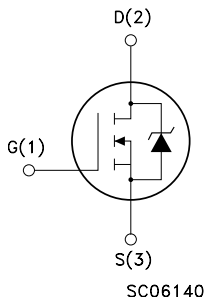
Description

The devices are realized with the second generation of MDmesh Technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB21NM50N	B21NM50N	D^2PAK	Tape & reel
STB21NM50N-1	B21NM50N	I^2PAK	Tube
STF21NM50N	F21NM50N	TO-220FP	Tube
STP21NM50N	P21NM50N	TO-220	Tube
STW21NM50N	W21NM50N	TO-247	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/ D^2PAK/ I^2PAK/TO-247	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	500		V
V_{GS}	Gate- source voltage	±25		V
I_D	Drain current (continuous) at T_C = 25°C	18	18(1)	A
I_D	Drain current (continuous) at T_C = 100°C	11	11(1)	A
I_{DM} (2)	Drain current (pulsed)	72	72(1)	A
P_{TOT}	Total dissipation at T_C = 25°C	140	30	W
	Derating factor	1.12	0.23	W/°C
dv/dt(3)	Peak diode recovery voltage slope	15		V/ns
Viso	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s;T_C=25°C)	--	2500	V
T_{stg}	Storage temperature	–55 to 150		°C
T_j	Max. operating junction temperature	150		

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤18 A, di/dt ≤400 A/µs, V_{DD} =80% $V_{(BR)DSS}$

Table 2. Thermal data

Symbol	Parameter	TO-220/D²PAK/ I²PAK / TO-247	TO-220FP	Unit
Rthj-case	Thermal resistance junction-case max	0.89	4.21	°C/W
Rthj-amb	Thermal resistance junction-ambient max	62.5		°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	9	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}, V_{DD} = 50V)	480	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS} = 0	500			V
dv/dt(1)	Drain source voltage slope	V_{DD}=400V, I_D=25A, V_{GS}=10V		44		V/ns
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating,T_C@125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 9A		0.150	0.190	Ω

1. Characteristic value at turn off on inductive load

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15V, I_D = 9A		12		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		1950 420 60		pF pF pF
$C_{oss\ eq.}$(2)	Equivalent output capacitance	V_{GS} = 0V, V_{DS} = 0V to 400V		270		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} =250V, I_D = 9A R_G = 4.7Ω V_{GS} = 10V		22 18 90 30		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 400V, I_D = 18A, V_{GS} = 10V,		65 10 30		nC nC nC
R_g	Gate input resistance	f=1MHz Gate DC Bias=0 test signal level=20mV open drain		1.6		Ω

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				18 72	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 18A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 18A, di/dt=100A/µs V_{DD} = 100V,		360 5 27		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 18A, di/dt=100A/µs V_{DD} = 100V, T_j = 150°C		464 6.5 27		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

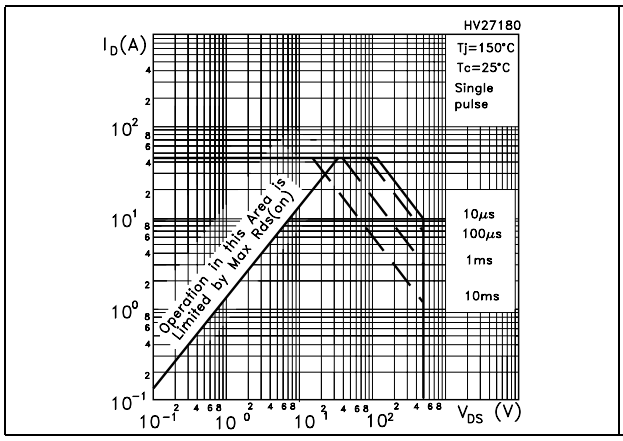


Figure 2. Thermal impedance

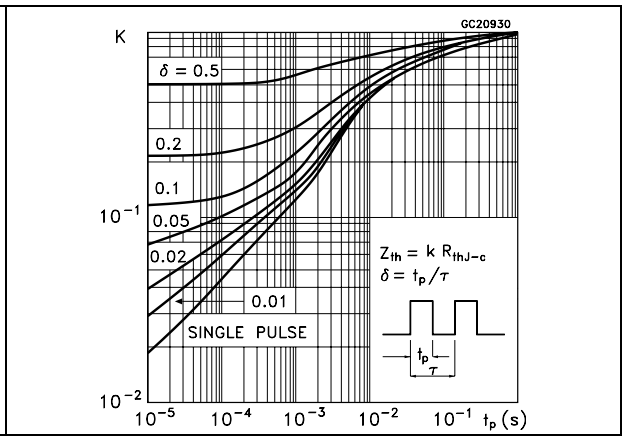


Figure 3. Safe operating area for TO-220FP

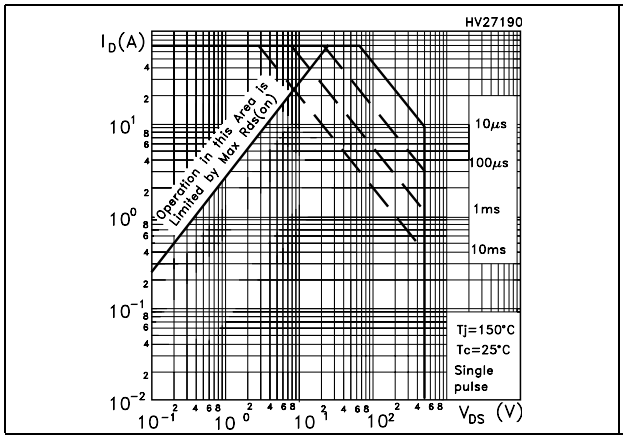


Figure 4. Thermal impedance for TO-220FP

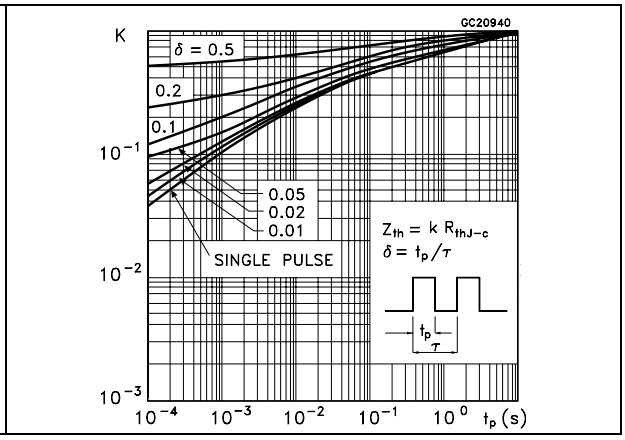


Figure 5. Output characteristics

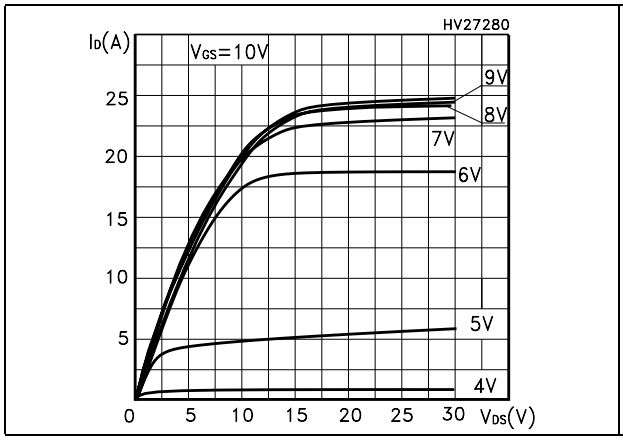


Figure 6. Transfer characteristics