STB20N65M5, STI20N65M5, STP20N65M5, STW20N65M5

N-channel 650 V, 0.160 Ω typ., 18 A MDmesh™ V Power MOSFET in D^2PAK, I^2PAK, TO-220 and TO-247 packages

Datasheet — production data

Features

Order codes	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D
STB20N65M5	710 V	0.19 Ω	18 A
STI20N65M5			
STP20N65M5			
STW20N65M5			

- Worldwide best $R_{DS(on)}$ * area
- Higher V_{DSS} rating and high dv/dt capability
- Excellent switching performance
- 100% avalanche tested

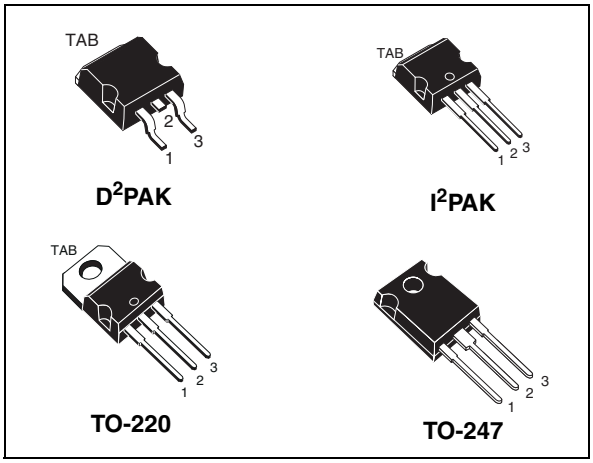
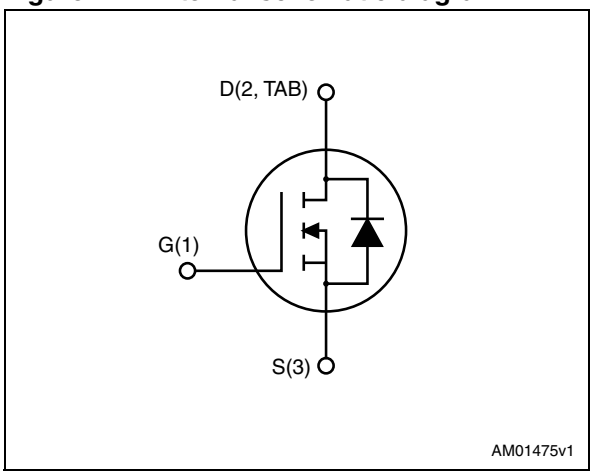


Figure 1. Internal schematic diagram



Applications

- Switching applications

Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB20N65M5	20N65M5	D^2PAK	Tape and reel
STI20N65M5		I^2PAK	Tube
STP20N65M5		TO-220	
STW20N65M5		TO-247	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	18	A
I_D	Drain current (continuous) at T_C = 100 °C	11.3	A
I_{DM} (1)	Drain current (pulsed)	72	A
P_{TOT}	Total dissipation at T_C = 25 °C	130	W
dv/dt (1)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. I_{SD} ≤ 18 A, di/dt ≤400 A/µs; V_{DS} peak < $V_{(BR)DSS}$, V_{DD}=400 V

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		D^2PAK	I^2PAK, TO-220	TO-247	
$R_{thj-case}$	Thermal resistance junction-case max	0.96			°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max		62.5	50	°C/W
$R_{thj-pcb}$(1)	Thermal resistance junction-pcb max	30			°C/W

1. When mounted on 1 inch² FR-4, 1 Oz copper board.

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetetive (pulse width limited by T_{jmax})	4	A
E_{AS}	Single pulse avalanche energy (starting t_j=25°C, I_d= I_{AR}; V_{dd}=50 V)	270	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 650 V V_{DS} = 650 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 9 A		0.160	0.19	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	1434 38 3.7	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0	-	118	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	35	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3.5	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 9 A, V_{GS} = 10 V	-	36 7.5 18	-	nC nC nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 12 A,	-	43	-	ns
$t_{r(v)}$	Voltage rise time	R_G = 4.7 Ω, V_{GS} = 10 V		7.5		ns
$t_{f(i)}$	Current fall time			7.5		ns
$t_{c(off)}$	Crossing time			11.5		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		18	A
I_{SDM} (1)	Source-drain current (pulsed)				72	A
V_{SD} (2)	Forward on voltage	I_{SD} = 18 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 18 A, di/dt = 100 A/µs	-	288		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V (see)		4		µC
I_{RRM}	Reverse recovery current			27		A
t_{rr}	Reverse recovery time	I_{SD} = 18 A, di/dt = 100 A/µs	-	342		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_j = 150 °C		4.7		µC
I_{RRM}	Reverse recovery current			28		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK, I²PAK, TO-220

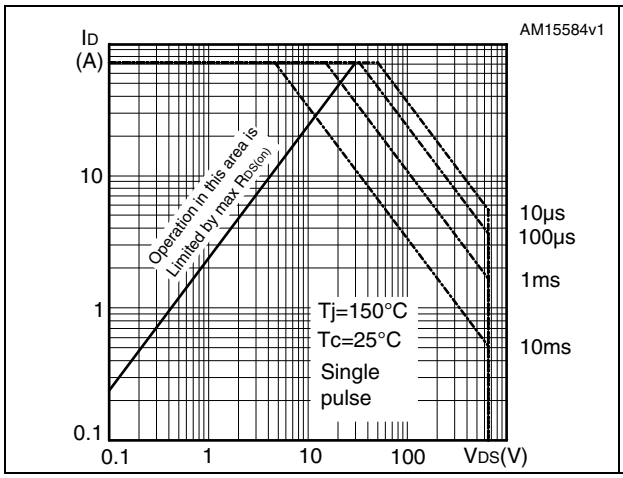


Figure 3. Thermal impedance for D²PAK, I²PAK, TO-220

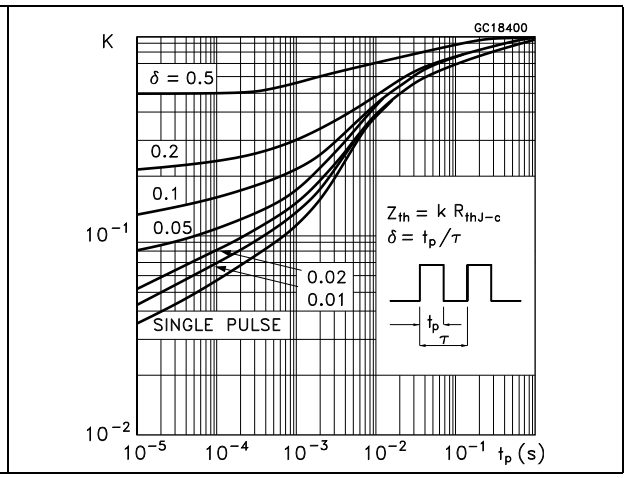


Figure 4. Safe operating area for TO-247

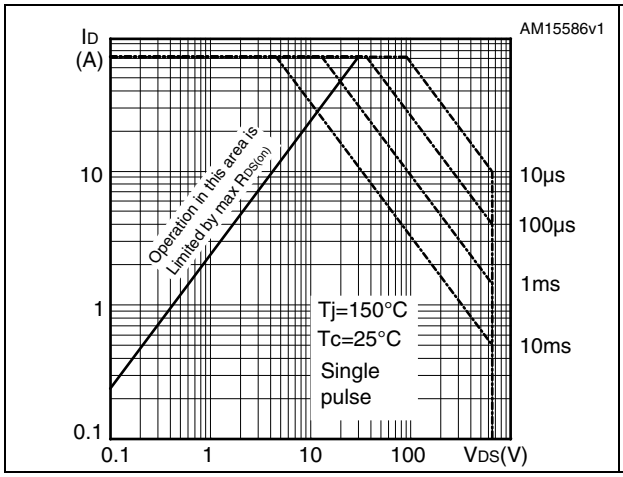


Figure 5. Thermal impedance for TO-247

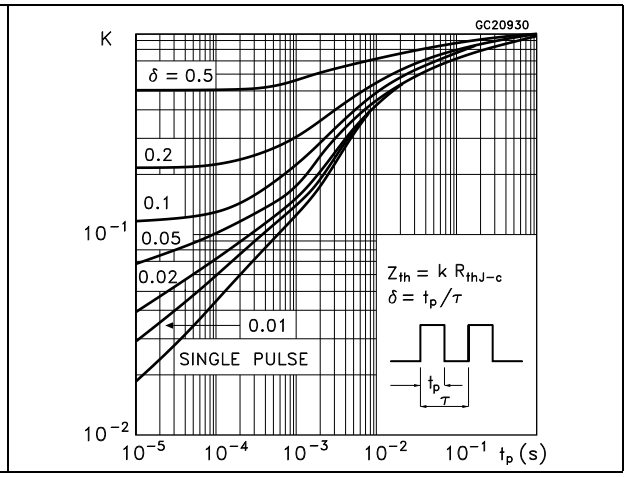


Figure 6. Output characteristics

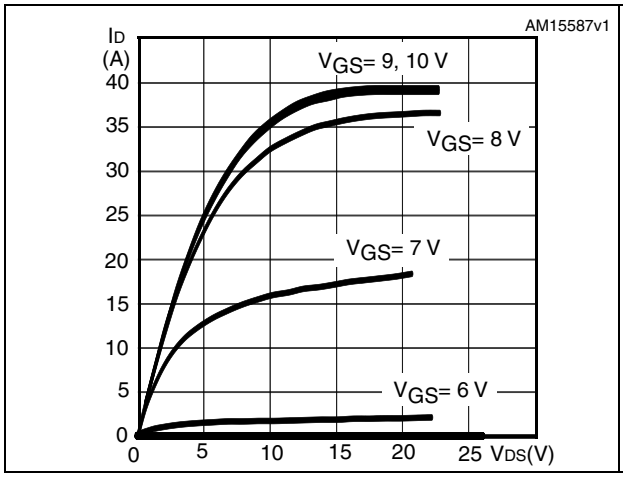


Figure 7. Transfer characteristics