



# STW18NB40 STH18NB40FI

N-CHANNEL 400V - 0.19  $\Omega$  - 18.4 A TO-247/ISOWATT218

PowerMesh™ MOSFET

PRELIMINARY DATA

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STW18NB40	400 V	< 0.26 $\Omega$	18.4 A
STH18NB40FI	400 V	< 0.26 $\Omega$	12.4 A

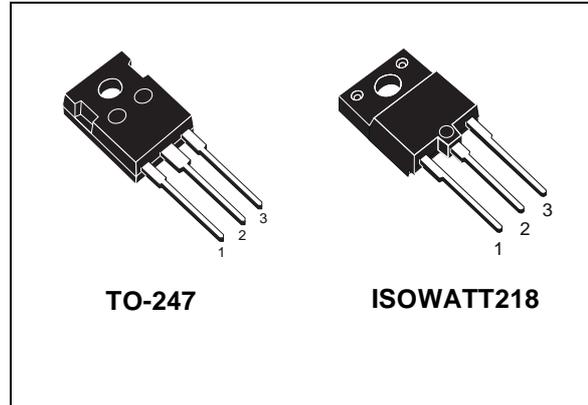
- TYPICAL R<sub>DS(on)</sub> = 0.19  $\Omega$
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

## DESCRIPTION

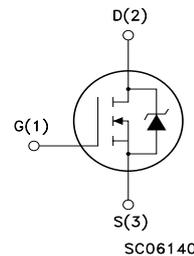
Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest R<sub>DS(on)</sub> per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

## APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT AND UNINTERRUPTIBLE POWER SUPPLIES AND MOTOR DRIVE



## INTERNAL SCHEMATIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STW18NB40	STH18NB40FI	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	400		V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	400		V
V <sub>GS</sub>	Gate- source Voltage	±30		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	18.4	12.4	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	11.6	7.8	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	73.6	73.6	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	190	80	W
	Derating Factor	1.52	0.64	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	4.5	4.5	V/ns
V <sub>ISO</sub>	Insulation Withstand Voltage (DC)	-	2000	V
T <sub>stg</sub>	Storage Temperature	-65 to 150		°C
T <sub>j</sub>	Max. Operating Junction Temperature	150		°C

(•)Pulse width limited by safe operating area

(1)I<sub>SD</sub><18.4A, di/dt<200A/ $\mu$ , V<sub>DD</sub><V<sub>(BR)DSS</sub>.T<sub>J</sub><T<sub>JMAX</sub>

## STW18NB40/STH18NB40FI

### THERMAL DATA

		TO-247	ISOWATT218	
Rthj-case	Thermal Resistance Junction-case Max	0.66	1.56	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	30		°C/W
Rthc-sink	Thermal Resistance Case-sink Typ	0.1		°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	300		°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	18.4	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	450	mJ

### ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	400			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 50	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3	4	5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 6.2 A		0.19	0.26	Ω
I <sub>D(on)</sub>	On State Drain Current	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , V <sub>GS</sub> = 10V	18.4			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , I <sub>D</sub> = 9.2 A		9.3		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		2480		pF
C <sub>oss</sub>	Output Capacitance			435		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			47		pF

## ELECTRICAL CHARACTERISTICS (CONTINUED)

## SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 200\text{ V}$ , $I_D = 9.2\text{ A}$ $R_G = 4.7\Omega$ , $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		27		ns
$t_r$	Rise Time			14		ns
$Q_g$	Total Gate Charge	$V_{DD} = 320\text{ V}$ , $I_D = 18.4\text{ A}$ , $V_{GS} = 10\text{ V}$		60	84	nC
$Q_{gs}$	Gate-Source Charge			16		nC
$Q_{gd}$	Gate-Drain Charge			28.3		nC

## SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 320\text{ V}$ , $I_D = 18.4\text{ A}$ , $R_G = 4.7\Omega$ , $V_{GS} = 10\text{ V}$ (see test circuit, Figure 5)		13		ns
$t_f$	Fall Time			15		ns
$t_c$	Cross-over Time			27		ns

## SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				18.4	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				73.6	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 18.4\text{ A}$ , $V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 18.4\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$ , $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		480		ns
$Q_{rr}$	Reverse Recovery Charge			5.5		$\mu\text{C}$
$I_{RRM}$	Reverse Recovery Current			23		A

Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.