STF15NM65N-STI15NM65N-STW15NM65N STB15NM65N-STP15NM65N

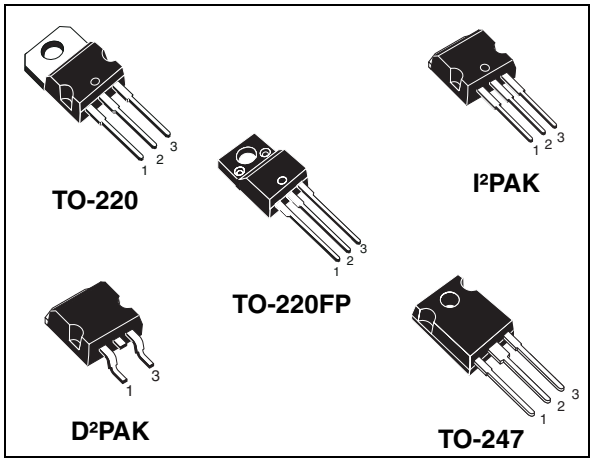
N-channel 650V - 0.25Ω - 15.5A - TO-220/FP - D^2/I^2PAK - TO-247
Second generation MDmesh™ Power MOSFET

Features

Type	V_{DSS} (@Tjmax)	$R_{DS(on)}$ Max	I_D
STB15NM65N	710 V	< 0.27 Ω	15.5 A
STF15NM65N	710 V	< 0.27 Ω	15.5 A(1)
STI15NM65N	710 V	< 0.27 Ω	15.5 A
STP15NM65N	710 V	< 0.27 Ω	15.5 A
STW15NM65N	710 V	< 0.27 Ω	15.5 A

1. Limited only by maximum temperature allowed

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Application

- Switching applications

Description

This series of devices implements the second generation of MDmesh™ Technology. This revolutionary Power MOSFET associates a new vertical structure to the Company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters

Figure 1. Internal schematic diagram

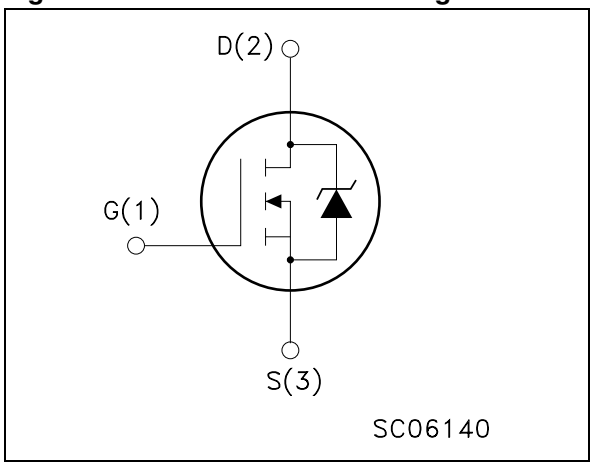


Table 1. Device summary

Order codes	Marking	Package	Packaging
STI15NM65N	15NM65N	I²PAK	Tube
STF15NM65N	15NM65N	TO-220FP	Tube
STP15NM65N	15NM65N	TO-220	Tube
STB15NM65NT4	15NM65N	D²PAK	Tape & reel
STW15NM65N	15NM65N	TO-247	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/I²PAK D²PAK/TO-247	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS}=0)	650		V
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at T_C = 25°C	15.5	15.5(1)	A
I_D	Drain current (continuous) at T_C = 100°C	10	10(1)	A
I_{DM} (2)	Drain current (pulsed)	62	62(1)	A
P_{TOT}	Total dissipation at T_C = 25°C	150	35	W
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s;T_C=25°C)	--	2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤15.5A, di/dt ≤400A/µs, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220/I²PAK D²PAK/TO-247	TO-220FP	
Rthj-case	Thermal resistance junction-case Max	0.83	3.6	°C/W
Rthj-amb	Thermal resistance junction-amb Max	62.5		°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max)	4	A
E_{AS}	Single pulse avalanche energy (starting Tj=25 °C, I_D= I_{AS}, V_{DD}= 50 V)	400	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
dv/dt (1)	Drain source voltage slope	Vdd=520 V, Id=15.5 A, Vgs=10 V		30		V/ns
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, @125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 7.75 A		0.25	0.27	Ω

1. Characteristics value at turn off on inductive load

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS}=15 V, I_D =7.75 A		15		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0		1900 110 10		pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0V to 520 V		230		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 15.5 A, V_{GS} = 10 V,		55 9 30		nC nC nC

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} =325 V, I_D = 7.75 A R_G = 4.7 Ω V_{GS} = 10 V		25 8 80 26		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				15.5 62	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 15.5 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 15.5 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 25 °C		460 6 27		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 15.5 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150°C		600 8 27		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220 - D²PAK - I²PAK

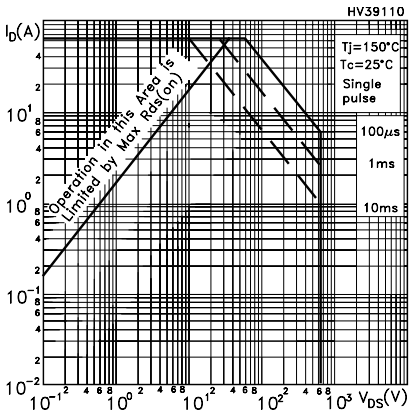


Figure 3. Thermal impedance for TO-220 - D²PAK - I²PAK

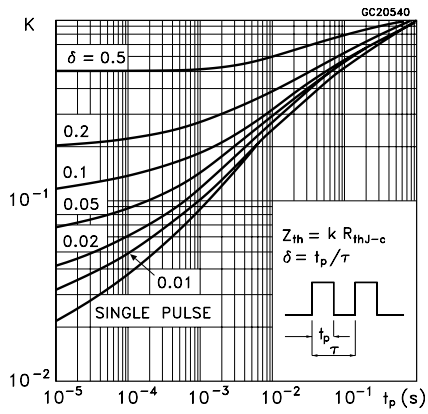


Figure 4. Safe operating area for TO-220FP

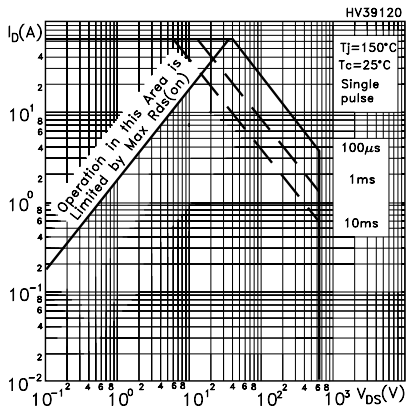


Figure 5. Thermal impedance for TO-220FP

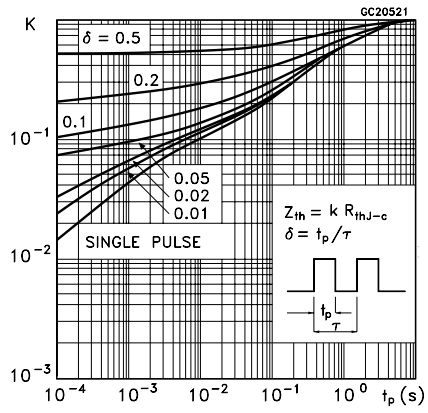


Figure 6. Safe operating area for TO-247

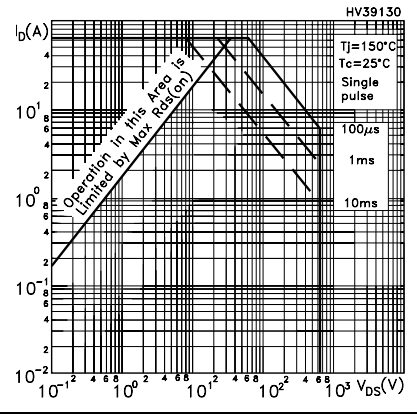


Figure 7. Thermal impedance for TO-247