

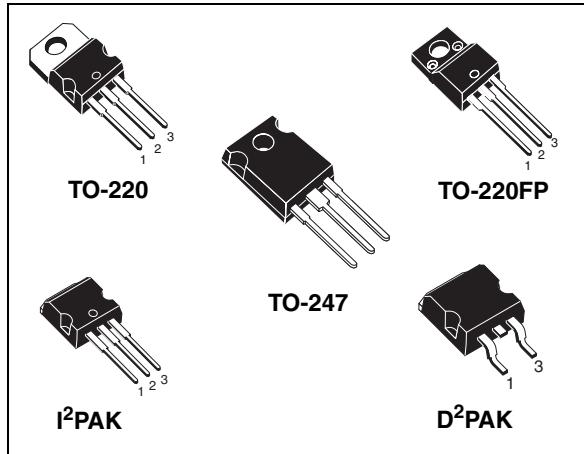
# STP15NK50Z/FP - STB15NK50Z STB15NK50Z-1 - STW15NK50Z

N-channel 500V - 0.30Ω - 14A TO-220/FP/D<sup>2</sup>PAK/I<sup>2</sup>PAK/TO-247  
Zener-protected SuperMESH™ Power MOSFET

## General features

Type	V <sub>DSS</sub>	R <sub>D(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STP15NK50Z	500V	<0.34Ω	14A	160 W
STP15NK50ZFP	500V	<0.34Ω	14A	40 W
STB15NK50Z	500V	<0.34Ω	14A	160W
STB15NK50Z-1	500V	<0.34Ω	14A	160W
STW15NK50Z	500V	<0.34Ω	14A	160W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



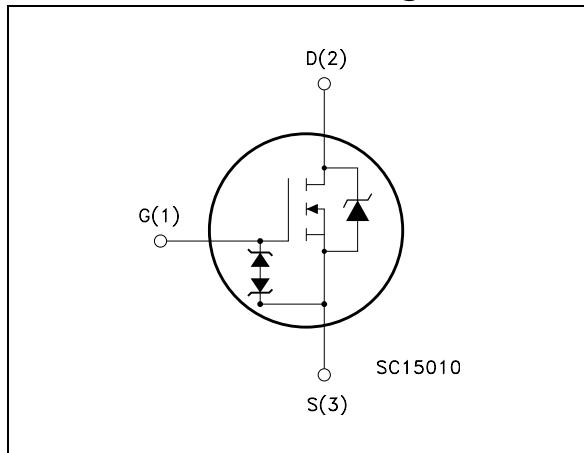
## Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

## Applications

- Switching application

## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STP15NK50Z	P15NK50Z	TO-220	Tube
STP15NK50ZFP	P15NK50ZFP	TO-220FP	Tube
STB15NK50ZT4	B15NK50Z	D <sup>2</sup> PAK	Tape & reel
STB15NK50Z	B15NK50Z	D <sup>2</sup> PAK	Tube
STB15NK50Z-1	B15NK50Z	I <sup>2</sup> PAK	Tube
STW15NK50Z	W15NK50Z	TO-247	Tube

# 1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/D <sup>2</sup> PAK I <sup>2</sup> PAK/TO-247	TO-220FP	
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	500		V
V <sub>DGR</sub>	Drain-gate voltage (R <sub>GS</sub> = 20KΩ)	500		V
V <sub>GS</sub>	Gate-source voltage	± 30		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25°C	14	14 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> =100°C	8.8	8.8 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	56	56 <sup>(1)</sup>	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25°C	160	40	W
	Derating Factor	1.28	0.32	W/°C
I <sub>GS</sub>	Gate-source current (DC)	± 20		mA
V <sub>esd(G-S)</sub>	G-S ESD (HBM C=100pF, R=1.5kΩ)	4000		kV
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	4.5		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s;T <sub>C</sub> =25°C)	--	2500	V
T <sub>J</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	-50 to 150°C		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I<sub>SD</sub> ≤ 4A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>

Table 2. Thermal data

Symbol	Parameter	Value				Unit
		TO-220 I <sup>2</sup> PAK	D <sup>2</sup> PAK	TO-220FP	TO-247	
R <sub>rthj-case</sub>	Thermal resistance junction-case Max	0.78		3.1	0.78	°C/W
R <sub>rthj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb max		60			°C/W

## Electrical ratings STP15NK50Z - STP15NK50ZFP - STB15NK50Z - STB15NK50Z-1 - STW15NK50Z

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**Table 2. Thermal data**

$R_{thj-a}$	Thermal resistance junction-ambient max	62.5	50	°C/W
$T_L$	Maximum lead temperature for soldering purpose	300		°C

1. When mounted on minimum foot-print

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ Max)	14	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25^\circ\text{C}$ , $I_d=I_{AR}$ , $V_{DD}=50\text{V}$ )	300	mJ

**Table 4. Gate-source zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{GS}=\pm 1\text{mA}$ (Open Drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2 Electrical characteristics

( $T_{CASE}=25^\circ\text{C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{mA}$ , $V_{GS} = 0$	500			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ , $V_{DS} = \text{Max rating } @ 125^\circ\text{C}$		1 50	$\mu\text{A}$ $\mu\text{A}$	
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\mu\text{A}$	3	3.75	4.5	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$ , $I_D = 7\text{A}$		0.30	0.34	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$ , $I_D = 7\text{A}$		12		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		2260 264 64		pF pF pF
$C_{oss\ eq}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$ , $V_{DS} = 0\text{V}$ to $400\text{V}$		150		pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 400\text{V}$ , $I_D = 14\text{A}$ $V_{GS} = 10\text{V}$		76 15 40	106	nC nC nC
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 250\text{ V}$ , $I_D = 7\text{A}$ , $R_G = 4.7\Omega$ , $V_{GS} = 10\text{V}$		20 23 62 15		ns ns ns ns

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

2.  $C_{oss\ eq}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Source drain diode**

<b>Symbol</b>	<b>Parameter</b>	<b>Test conditions</b>	<b>Min</b>	<b>Typ.</b>	<b>Max</b>	<b>Unit</b>
$I_{SD}$	Source-drain current			14		A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)			56		A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=14A, V_{GS}=0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=14A,$ $di/dt = 100A/\mu s,$ $V_{DD}=29V, T_j=150^\circ C$		428 4.2 20		ns $\mu C$ A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%