STB150NF55
STP150NF55 - STW150NF55

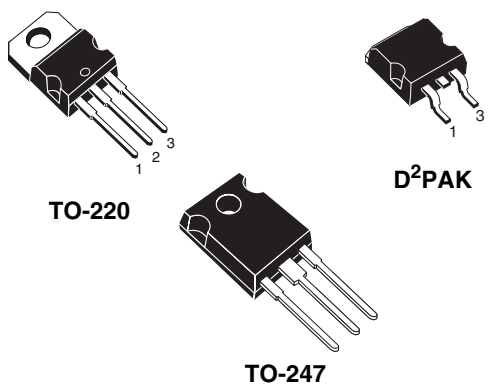
N-channel 55V - 0.005Ω - 120A - D^2PAK/TO-220/TO-247
STripFET™ II Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STB150NF55	55V	<0.006Ω	120A(1)
STP150NF55	55V	<0.006Ω	120A(1)
STW150NF55	55V	<0.006Ω	120A(1)

1. Current limited by package

- 100% avalanche tested



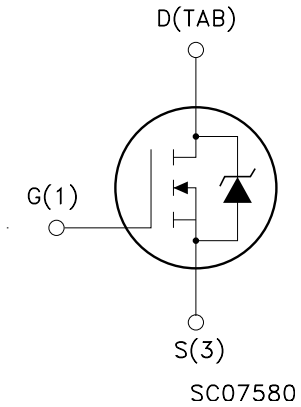
Description

This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

- Switching application

Internal schematic diagram



Order codes

Sales type	Marking	Package	Packaging
STB150NF55T4	B150NF55	D^2PAK	Tape & reel
STP150NF55	P150NF55	TO-220	Tube
STW150NF55	W150NF55	TO-247	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	55	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	55	V
V_{GS}	Gate- source voltage	± 20	V
I_D(1)	Drain current (continuous) at T_C = 25°C	120	A
I_D(1)	Drain current (continuous) at T_C = 100°C	106	A
I_{DM}(2)	Drain current (pulsed)	480	A
P_{tot}	Total dissipation at T_C = 25°C	300	W
	Derating Factor	2	W/°C
dv/dt (3)	Peak diode recovery voltage slope	8	V/ns
E_{AS} (4)	Single pulse avalanche energy	850	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		

1. Value limited by wire bonding
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 120A$, di/dt $\leq 200A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $Tj \leq T_{JMAX}$
4. Starting T_j = 25 °C, I_D = 60A, V_{DD} = 30V

Table 2. Thermal data

		TO-220	D^2PAK	TO-247	
Rthj-case	Thermal resistance junction-case max	0.5			°C/W
Rthj-amb	Thermal resistance junction-ambient max	62.5	--	50	°C/W
Rthj-pcb	Thermal resistance junction-pcb max	see			°C/W
T_J	Maximum lead temperature for soldering purpose(1)	300			°C

1. for 10 sec. 1.6mm from case

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} =0	55			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max ratings V_{DS} = max ratings, T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 60A		0.005	0.006	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15V, I_D = 60A		160		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0		4400 1050 350		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 27.5V, I_D = 60A R_G = 4.7Ω V_{GS} = 10V		35 180 140 80		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 27.5V, I_D = 120A, V_{GS} = 10V		140 35 70	190	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				120 480	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 120A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 120A, di/dt = 100A/µs, V_{DD} = 25V, T_j = 150°C		130 350 7.5		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

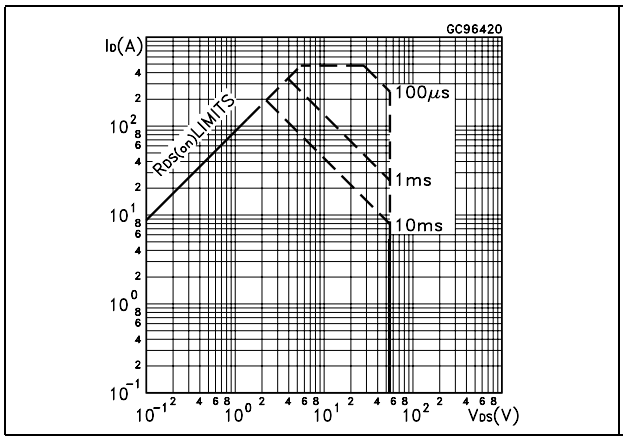


Figure 2. Thermal impedance

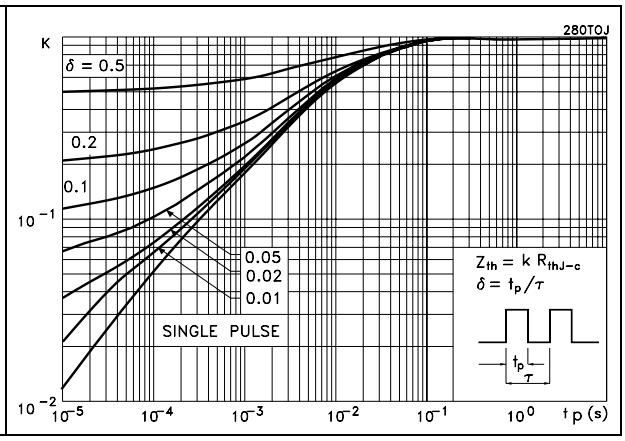


Figure 3. Output characterisics

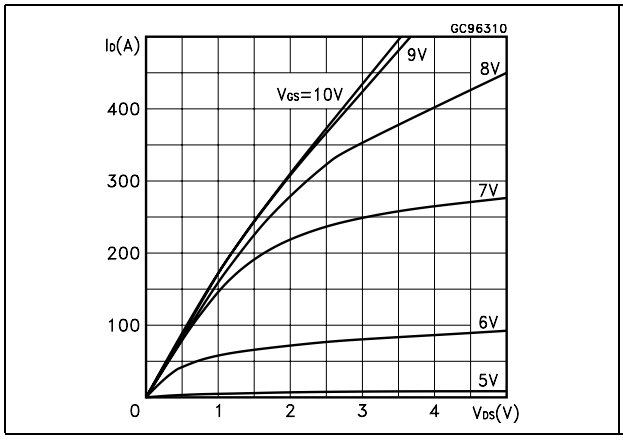


Figure 4. Transfer characteristics

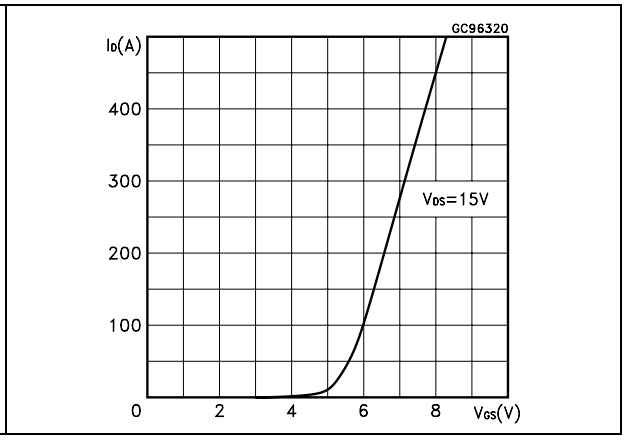


Figure 5. Transconductance

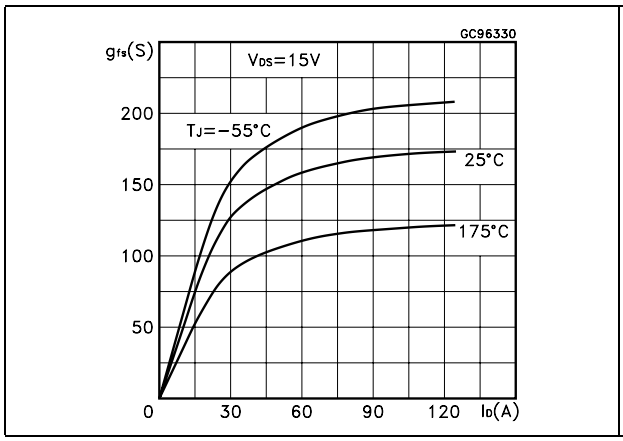


Figure 6. Static drain-source on resistance

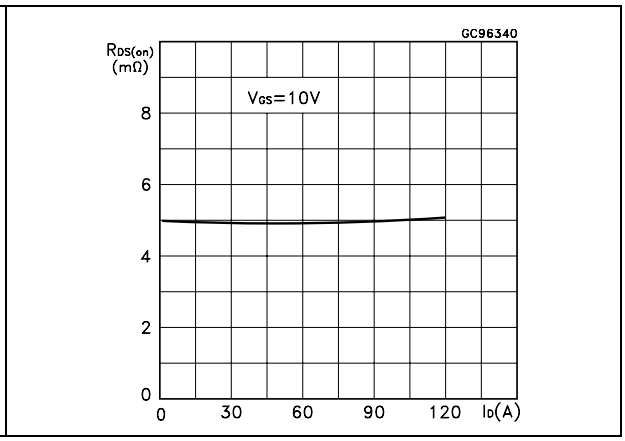


Figure 7. Gate charge vs gate-source voltage

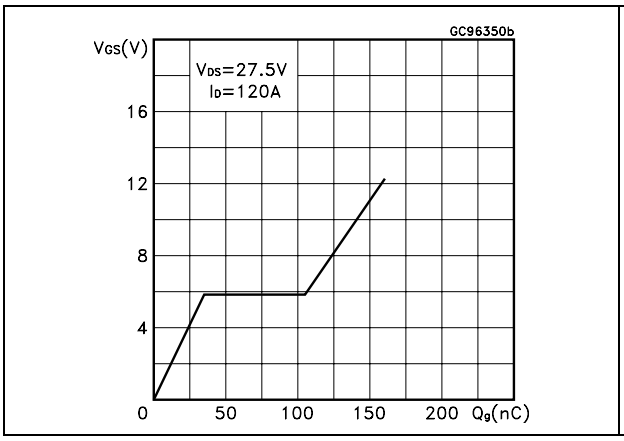


Figure 8. Capacitance variations

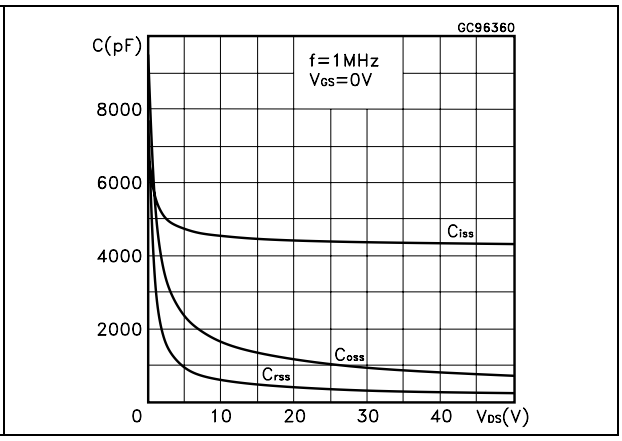


Figure 9. Normalized gate threshold voltage vs temperature

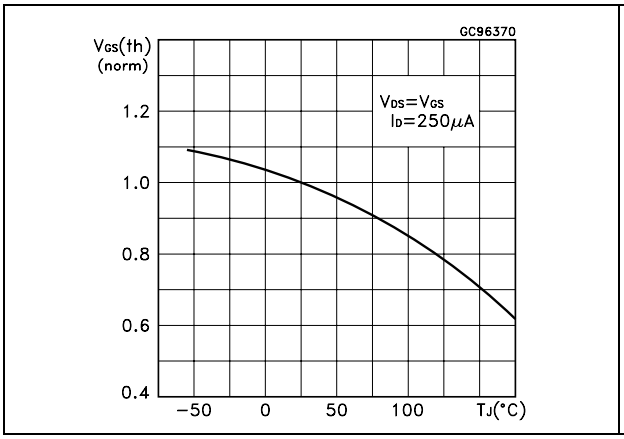


Figure 10. Normalized on resistance vs temperature

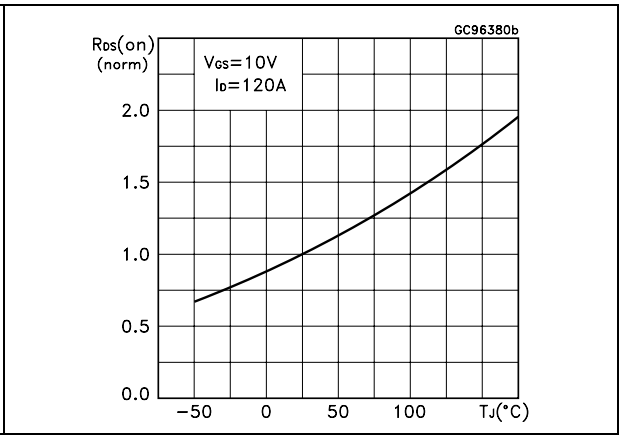


Figure 11. Source-drain diode forward characteristics

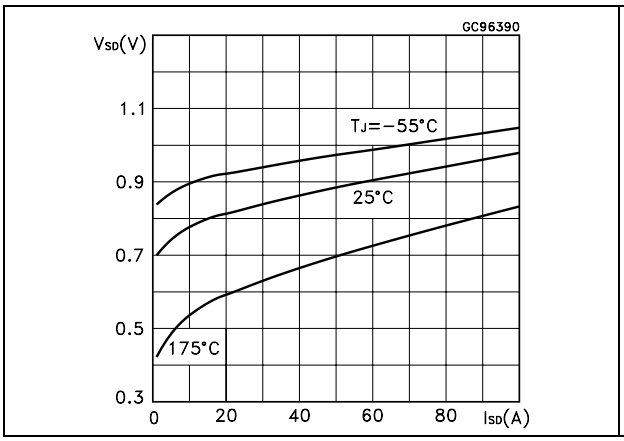


Figure 12. Normalized B_{VDSS} vs temperature