STF13N95K3, STFI13N95K3, STP13N95K3, STW13N95K3

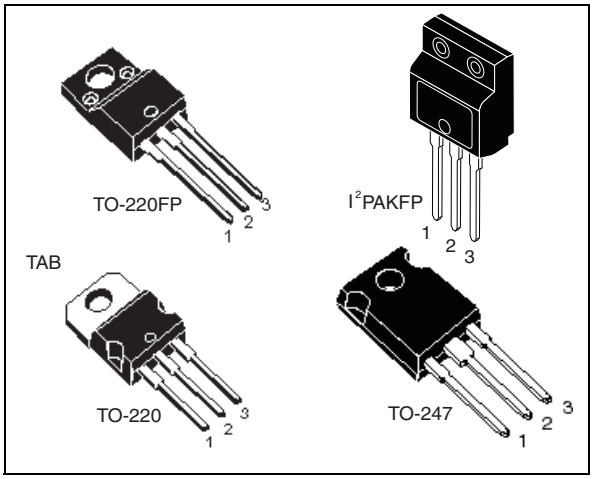
N-channel 950 V, 0.68 Ω typ., 10 A Zener-protected SuperMESH3™ Power MOSFET in TO-220FP, I²PAKFP, TO-220 and TO-247

Datasheet — production data

Features

Order codes	V_{DSS}	$R_{DS(on)}$max	I_D	P_{TOT}
STF13N95K3	950 V	< 0.85 Ω	10 A	40 W
STFI13N95K3				
STP13N95K3				190 W
STW13N95K3				

- Gate charge minimized
- Extremely large avalanche performance
- 100% avalanche tested
- Very low intrinsic capacitance
- Zener-protected



Applications

- Switching applications

Description

These SuperMESH3™ Power MOSFETs are the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

Figure 1. Internal schematic diagram

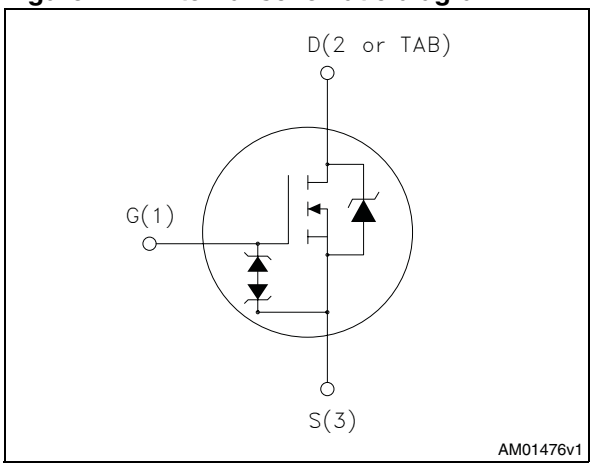


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF13N95K3	13N95K3	TO-220FP	Tube
STFI13N95K3		I²PAKFP	
STP13N95K3		TO-220	
STW13N95K3		TO-247	

1 Electrical ratings

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Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220 TO-247	TO-220FP I^2PAKFP	
V_{DS}	Drain source voltage	950		V
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25 °C	10	10 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	6	6 (1)	A
I_{DM} (2)	Drain current (pulsed)	40	40 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	190	40	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax})	13		A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V)	400		mJ
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; TC = 25 °C)		2500	V
dv/dt (3)	Peak diode recovery voltage slope	9		V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	- 55 to 150		°C

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. I_{SD} ≤ 10 A, di/dt ≤ 400 A/µs, V_{Peak} ≤$V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220	TO-247	TO-220FP I^2PAKFP	
Rthj-case	Thermal resistance junction-case max	0.66		3.13	°C/W
Rthj-amb	Thermal resistance junction-amb max	62.5	50	62.5	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	950			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 950V, V_{DS} = 950V, Tc=125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 5 A		0.68	0.85	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =100 V, f=1 MHz, V_{GS}=0	-	1620	-	pF
C_{oss}	Output capacitance			117		pF
C_{rss}	Reverse transfer capacitance			1.2		pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 760 V	-	115	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	131	-	pF
R_G	Intrinsic gate resistance	f = 1MHz open drain	-	2.3	-	Ω
Q_g	Total gate charge	V_{DD} = 760 V, I_D = 10 A	-	51	-	nC
Q_{gs}	Gate-source charge	V_{GS} =10 V		10		nC
Q_{gd}	Gate-drain charge			30		nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 475 V, I_D = 5 A, R_G=4.7 Ω, V_{GS}=10 V	-	18 16 50 21	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)		-		10 40	mA A
V_{SD}(1)	Forward on voltage	I_{SD}= 10 A, V_{GS}=0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 10 A, V_{DD}= 60 V di/dt = 100 A/µs,	-	500 9 36		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 10 A,V_{DD}= 60 V di/dt=100 A/µs, Tj=150 °C*(see*	-	624 11 37		ns µC A

1. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs ± 1mA, (open drain)	30	-		V

The built-in-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP and I²PAKFP

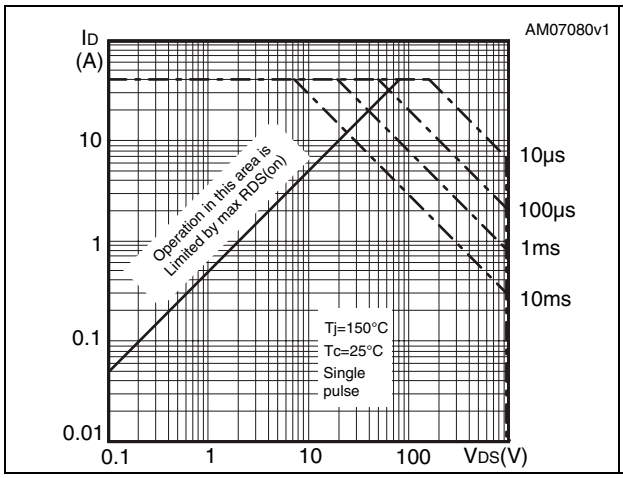

Figure 3. Thermal impedance for TO-220FP and I²PAKFP

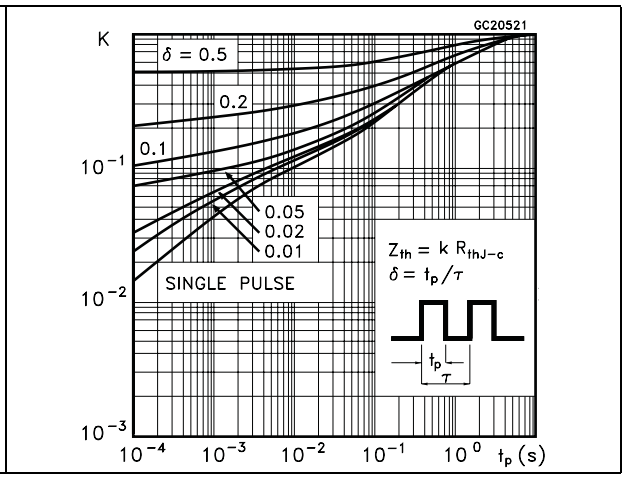

Figure 4. Safe operating area for TO-220

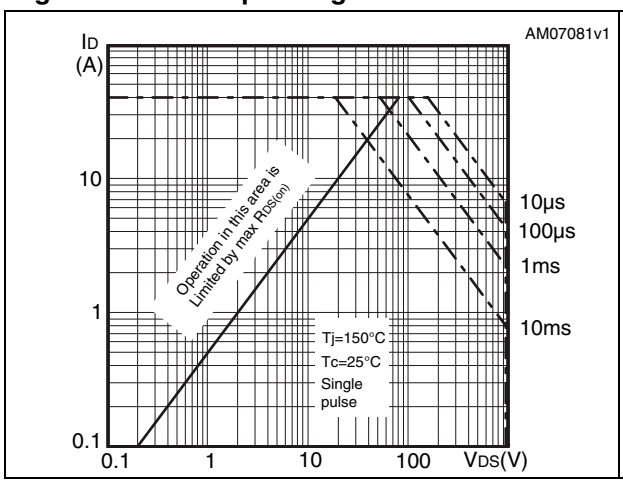

Figure 5. Thermal impedance for TO-220

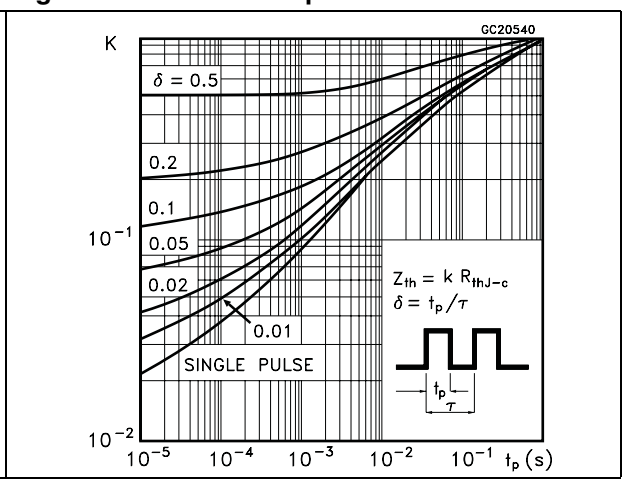

Figure 6. Safe operating area for TO-247

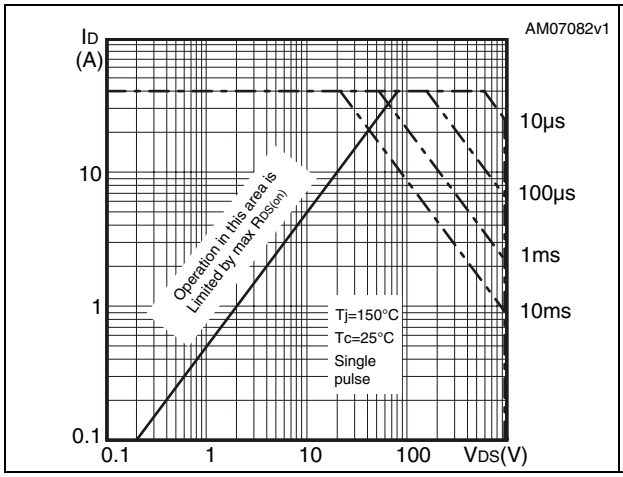

Figure 7. Thermal impedance for TO-247