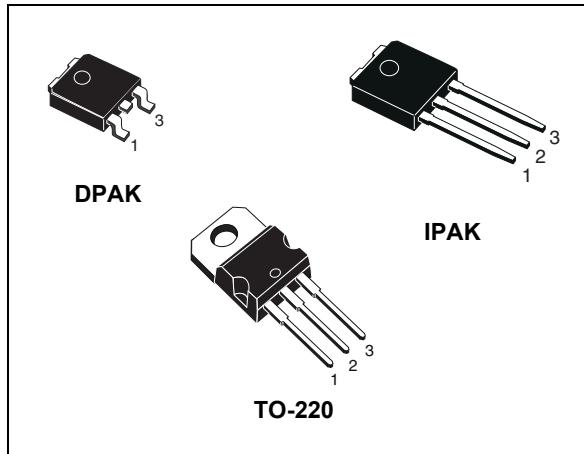


## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STD95N2LH5	25 V	< 0.0045 Ω	80 A
STP95N2LH5	25 V	< 0.0049 Ω	80 A
STU95N2LH5	25 V	< 0.0049 Ω	80 A

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- High avalanche ruggedness
- Low gate drive power losses



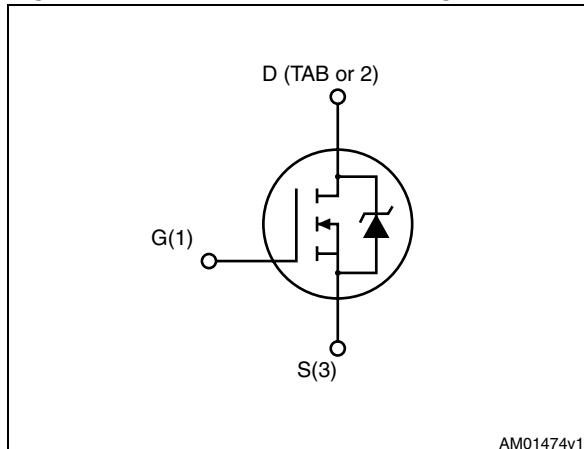
## Application

- Switching applications

## Description

This STripFET™V Power MOSFET technology is among the latest improvements, which have been especially tailored to achieve very low on-state resistance providing also one of the best-in-class FOM (figure of merit).

**Figure 1. Internal schematic diagram**



**Table 1. Device summary**

Order codes	Marking	Package	Packaging
STD95N2LH5	95N2LH5	DPAK	Tape and reel
STP95N2LH5	95N2LH5	TO-220	Tube
STU95N2LH5	95N2LH5	I <sup>PAK</sup>	Tube

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		DPAK/IPAK	TO-220	
$V_{DS}$	Drain-source voltage ( $V_{GS}=0$ )	25		V
$V_{GS}$	Gate-Source voltage	$\pm 22$		V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	80	95	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	67		A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	380	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	70	80	W
	Derating factor	0.47		W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	165		mJ
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 175		$^\circ\text{C}$

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting  $T_j = 25^\circ\text{C}$ ,  $I_d = 40 \text{ A}$ ,  $V_{dd} = 20 \text{ V}$

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.14	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-case max	100	$^\circ\text{C/W}$
$T_j$	Maximum lead temperature for soldering purpose	275	$^\circ\text{C}$

## 2 Electrical characteristics

( $T_{CASE}=25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0$	25			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 25\text{ V}$ $V_{DS} = 25\text{ V}, T_c = 125\text{ }^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 22\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 40\text{ A}$ SMD version		0.0038	0.0045	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 40\text{ A}$		0.0044	0.0049	$\Omega$
		$V_{GS} = 5\text{ V}, I_D = 40\text{ A}$ SMD version		0.005	0.006	$\Omega$
		$V_{GS} = 5\text{ V}, I_D = 40\text{ A}$		0.006	0.007	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance					pF
$C_{oss}$	Output capacitance					pF
$C_{rss}$	Reverse transfer capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	1817 420 67	-	pF
$Q_g$	Total gate charge					nC
$Q_{gs}$	Gate-source charge	$V_{DD} = 13\text{ V}, I_D = 80\text{ A}$	-	13.4	-	nC
$Q_{gd}$	Gate-drain charge	$V_{GS} = 5\text{ V}$	-	6.7	-	nC
$Q_{gs1}$	Pre $V_{th}$ gate-to-source charge	$V_{DD} = 13\text{ V}, I_D = 80\text{ A}$	-	3.5	-	nC
$Q_{gs2}$	Post $V_{th}$ gate-to-source charge		-	3.2	-	nC
$R_G$	Gate input resistance	$f = 1\text{ MHz}$ gate bias Bias = 0 test signal level = 20 mV open drain	-	1.1	-	$\Omega$

**Table 6. Switching on/off (inductive load)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=12.5\text{ V}$ , $I_D=40\text{ A}$ , $R_G=4.7\Omega$ , $V_{GS}=10\text{ V}$	-	7 38	-	ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD}=12.5\text{ V}$ , $I_D=40\text{ A}$ , $R_G=4.7\Omega$ , $V_{GS}=10\text{ V}$	-	22 7	-	ns ns

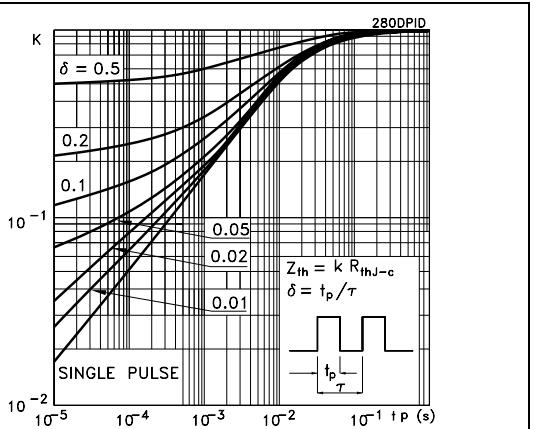
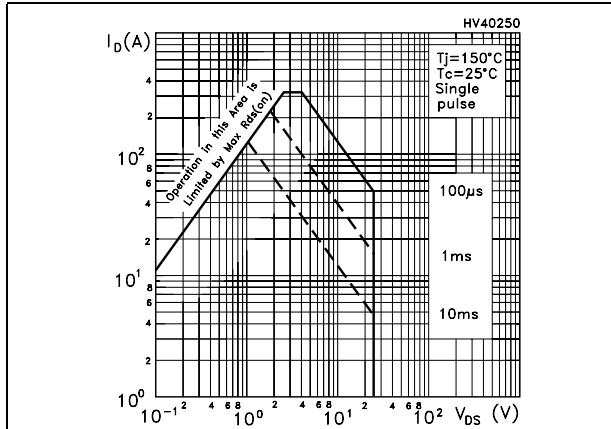
**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)		-		80 320	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=35\text{ A}$ , $V_{GS}=0$	-		1.1	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=80\text{ A}$ , $V_{DD}=20\text{ V}$ $di/dt=100\text{ A}/\mu\text{s}$ ,	-	32.4 27.1 1.7		ns nC A

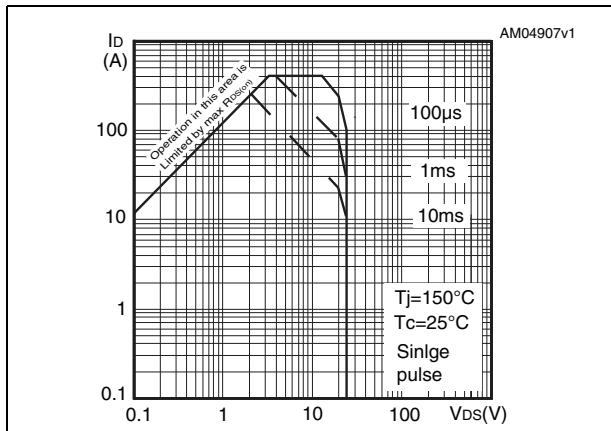
1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2.** Safe operating area for DPAK, IPAK



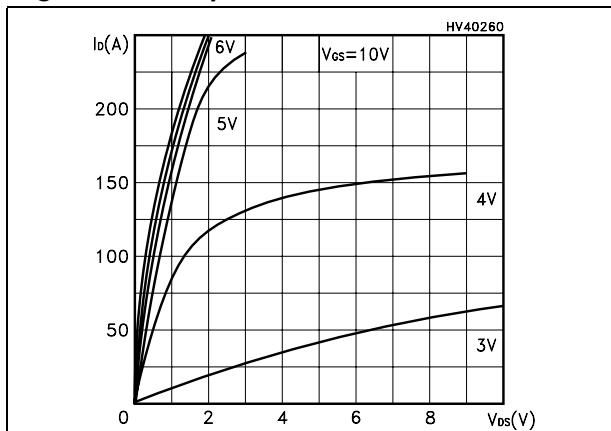
**Figure 4.** Safe operating area for TO-220



**Figure 5.** Thermal impedance for TO-220



**Figure 6.** Output characteristics



**Figure 7.** Transfer characteristics

