STD7N80K5, STP7N80K5, STU7N80K5

N-channel 800 V, 0.95 Ω typ., 6 A Zener-protected SuperMESH™ 5 Power MOSFETs in DPAK, TO-220 and IPAK packages

Datasheet - production data

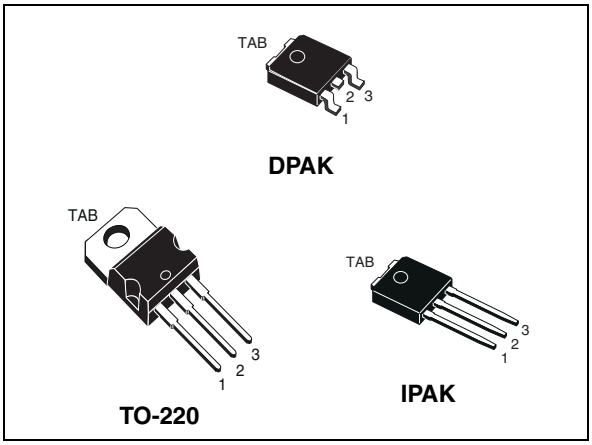
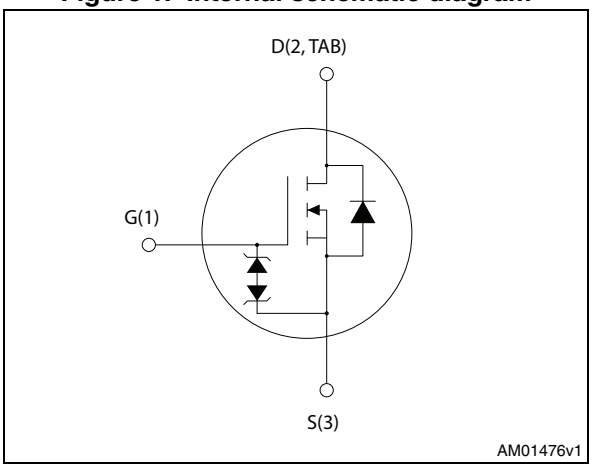


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$max	I_D	P_{TOT}
STD7N80K5	800 V	1.2 Ω	6 A	110 W
STP7N80K5				
STU7N80K5				

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These N-channel Zener-protected Power MOSFETs are designed using ST's revolutionary avalanche-rugged very high voltage SuperMESH™ 5 technology, based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance, and ultra-low gate charge for applications which require superior power density and high efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD7N80K5	7N80K5	DPAK	Tape and reel
STP7N80K5		TO-220	Tube
STU7N80K5		IPAK	

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	6	A
I_D	Drain current (continuous) at T_C = 100 °C	3.8	A
I_{DM} (1)	Drain current (pulsed)	24	A
P_{TOT}	Total dissipation at T_C = 25 °C	110	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax})	2	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V)	88	mJ
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
T_j	Operating junction temperature	-55 to 150	°C
T_{stg}	Storage temperature		°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 6$ A, di/dt $\leq$ 100 A/µs, $V_{DS(peak)} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		DPAK	TO-220	IPAK	
$R_{thj-case}$	Thermal resistance junction-case max	1.14			°C/W
$R_{thj-amb}$	Thermal resistance junction-amb max		62.5	100	°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-pcb max	50			°C/W

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS}= 0)	I_D = 1 mA	800			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 800 V V_{DS} = 800 V, Tc=125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 3 A		0.95	1.2	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =100 V, f=1 MHz, V_{GS}=0	-	360	-	pF
C_{oss}	Output capacitance		-	30	-	pF
C_{rss}	Reverse transfer capacitance		-	1	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 640 V	-	47	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	20	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0	-	6	-	Ω
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 6 A V_{GS} =10 V	-	13.4	-	nC
Q_{gs}	Gate-source charge		-	3.7	-	nC
Q_{gd}	Gate-drain charge		-	7.5	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 3 A, R_G=4.7 Ω, V_{GS}=10 V	-	11.3	-	ns
t_r	Rise time			8.3		ns
$t_{d(off)}$	Turn-off delay time			23.7		ns
t_f	Fall time			20.2		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
I_{SDM}	Source-drain current (pulsed)		-		24	A
V_{SD}(1)	Forward on voltage	I_{SD}= 6 A, V_{GS}=0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD}= 6 A, V_{DD}= 60 V di/dt = 100 A/µs,	-	315		ns
Q_{rr}	Reverse recovery charge		-	2.8		µC
I_{RRM}	Reverse recovery current		-	17.5		A
t_{rr}	Reverse recovery time	I_{SD}= 6 A,V_{DD}= 60 V di/dt=100 A/µs, Tj=150 °C	-	480		ns
Q_{rr}	Reverse recovery charge		-	3.8		µC
I_{RRM}	Reverse recovery current		-	16		A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}= ± 1mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK and IPAK

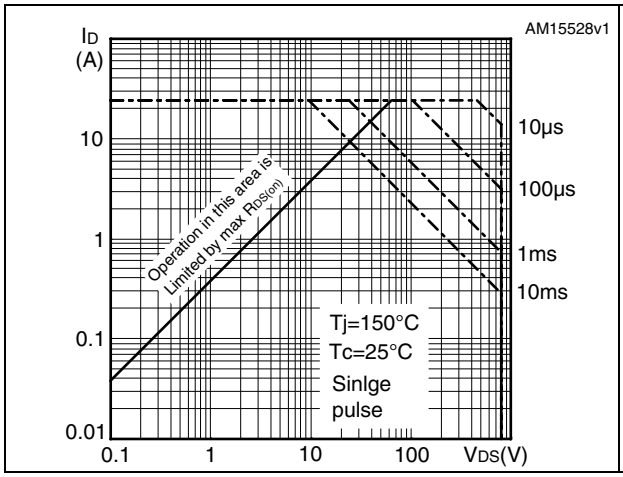


Figure 3. Thermal impedance for DPAK and IPAK

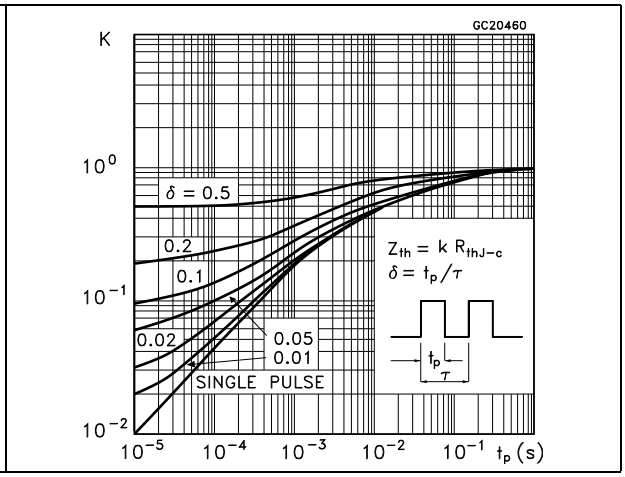


Figure 4. Safe operating area for TO-220

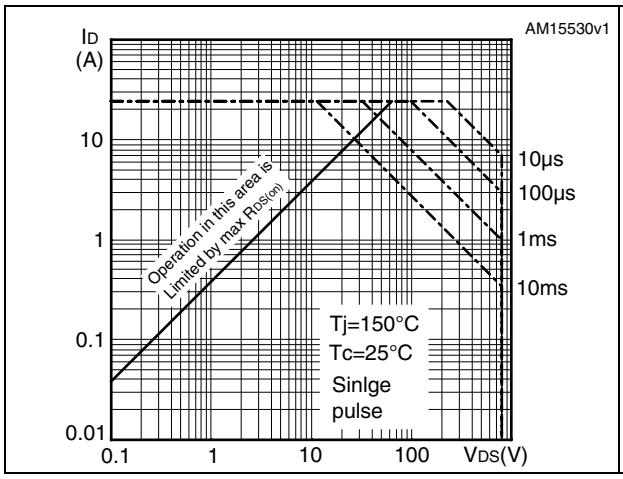


Figure 5. Thermal impedance for TO-220

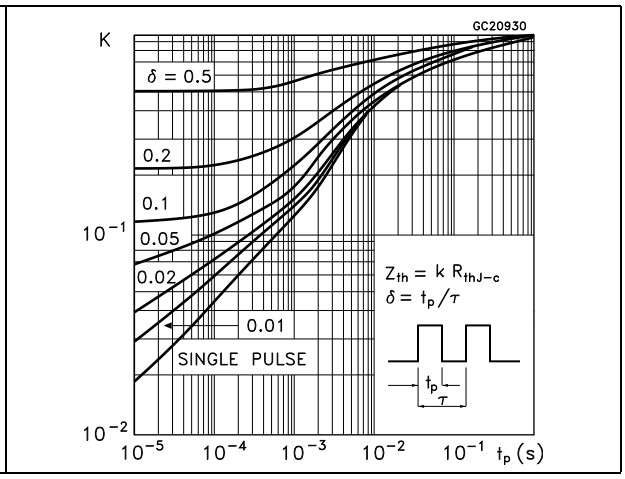


Figure 6. Output characteristics

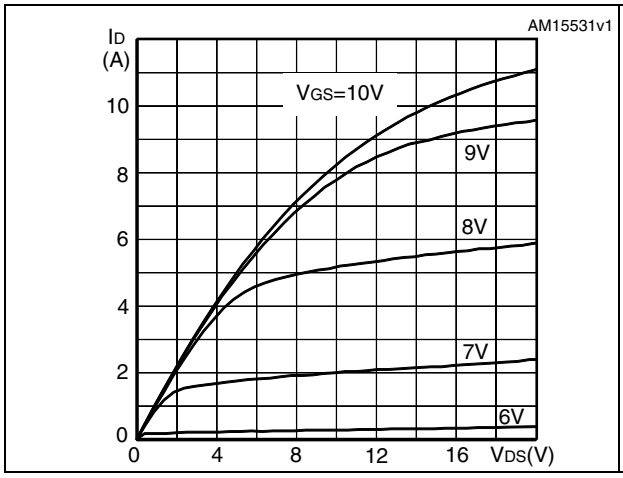


Figure 7. Transfer characteristics