

N-CHANNEL 800V -0.9Ω - 7.5A TO-220/TO-220FP

Zener-Protected SuperMESH™MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{D(on)}	I _D	P _w
STP9NK80Z	800 V	<1.2 Ω	7.5 A	150 W
STF9NK80Z	800 V	<1.2 Ω	7.5 A	35 W

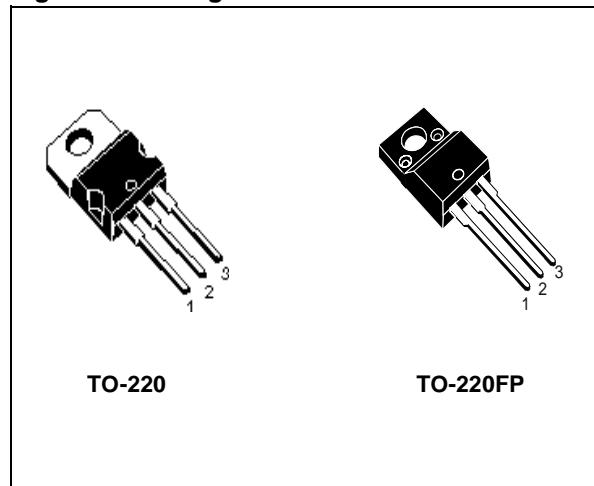
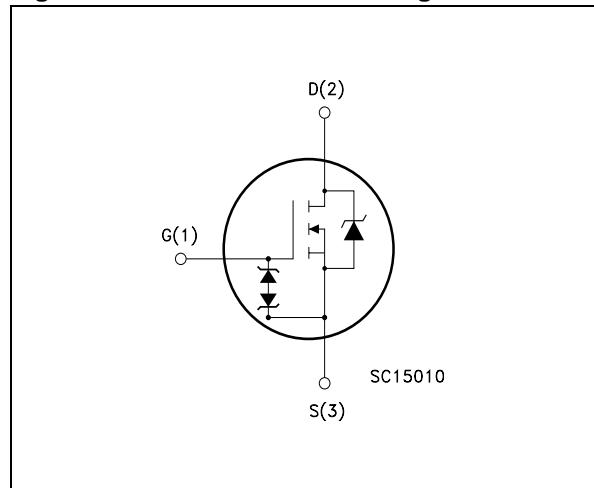
- TYPICAL R_{D(on)} = 0.9Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- IMPROVED ESD CAPABILITY
- 100% AVALANCHE RATED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES
- SMPS

Figure 1: Package

Figure 2: Internal Schematic Diagram

Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP9NK80Z	P9NK80Z	TO-220	TUBE
STF9NK80Z	F9NK80Z	TO-220FP	TUBE

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V _{DS}	Drain-source Voltage ($V_{GS} = 0$)	800		V
V _{DGR}	Drain-gate Voltage ($R_{GS} = 20 \text{ k}\Omega$)	800		V
V _{GS}	Gate- source Voltage	± 30		V
I _D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	7.5	7.5 (*)	A
I _D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	4.7	4.7 (*)	A
I _{DM} (•)	Drain Current (pulsed)	30	30 (*)	A
P _{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	150	35	W
	Derating Factor	1.20	0.28	W/°C
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	4000		V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5		V/ns
V _{ISO}	Insulation Withstand Voltage (DC)	-	2500	V
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-55 to 150 -55 to 150		°C °C

(•) Pulse width limited by safe operating area

(1) $I_{SD} \leq 7.5\text{A}$, $dV/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} = 80\%$ $V_{(BR)DSS}$

(*) Limited only by maximum temperature allowed

Table 4: Thermal Data

		TO-220	TO-220FP	
R _{thj-case}	Thermal Resistance Junction-case Max	0.83	3.6	°C/W
R _{thj-amb} T _I	Thermal Resistance Junction-ambient Max Maximum Lead Temperature For Soldering Purpose	62.5 350		°C/W °C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	7.5	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	350	mJ

Table 6: Gate-Source Zener Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	I _{GS} =± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)**Table 7: On/Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0	800			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 100μA	3	3.75	4.5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 3.75 A		0.9	1.2	Ω

Table 8: DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _f (1)	Forward Transconductance	V _{DS} = 15 V, I _D = 3.75 A		7.5		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		1900 180 38		pF pF pF
C _{oss} eq. (3)	Equivalent Output Capacitance	V _{GS} = 0V, V _{DS} = 0V to 640V		75		pF
t _{d(on)} t _r t _{d(off)} t _f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V _{DD} = 400 V, I _D = 3.75 A R _G = 4.7Ω V _{GS} = 10 V (see Figure 19)		26 19 58 18		ns ns ns ns
t _{r(Voff)} t _f t _c	Off-voltage Rise Time Fall Time Cross-over Time	V _{DD} = 640 V, I _D = 7.5A, R _G = 4.7Ω, V _{GS} = 10V (see Figure 20)		12 10 24		ns ns ns
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 640V, I _D = 7.5 A, V _{GS} = 10V (see Figure 22)		60 12 35	84	nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{SD} I _{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				7.5 30	A A
V _{SD} (1)	Forward On Voltage	I _{SD} = 7.5 A, V _{GS} = 0			1.6	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 7.5 A, di/dt = 100A/μs V _{DD} = 35V, T _j = 25°C (see Figure 20)		530 4.5 17		ns μC A
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 7.5 A, di/dt = 100A/μs V _{DD} = 35V, T _j = 150°C (see Figure 20)		690 6.4 17		ns μC A

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

3. C_{oss} eq. is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Figure 3: Safe Operating Area for TO-220

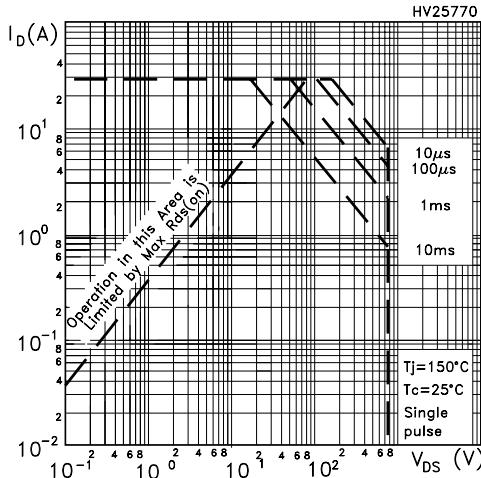


Figure 4: Safe Operating Area for TO-220FP

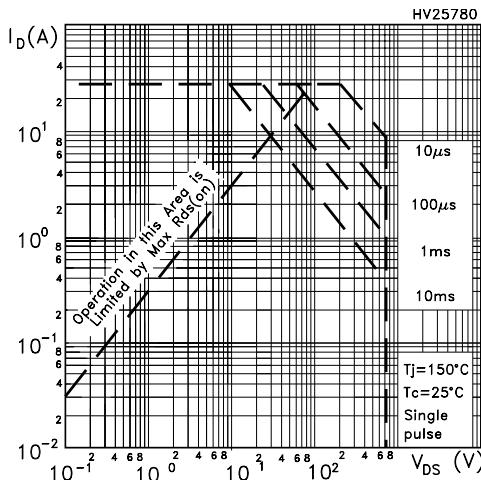


Figure 5: Output Characteristics

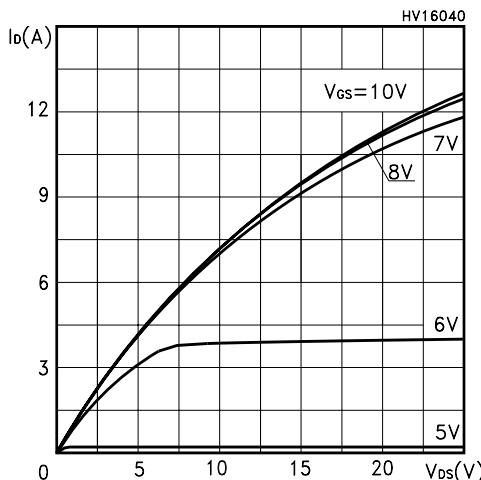


Figure 6: Thermal Impedance for TO-220

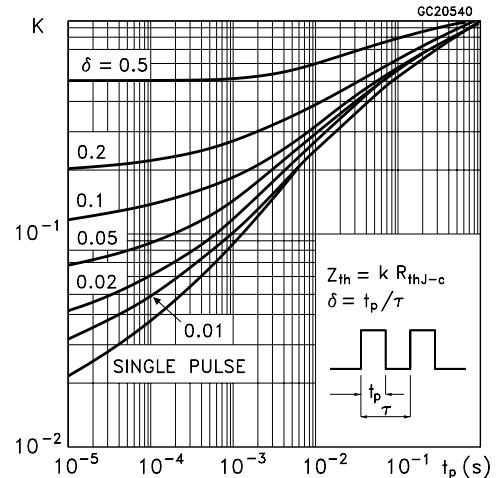


Figure 7: Thermal Impedance for TO-220FP

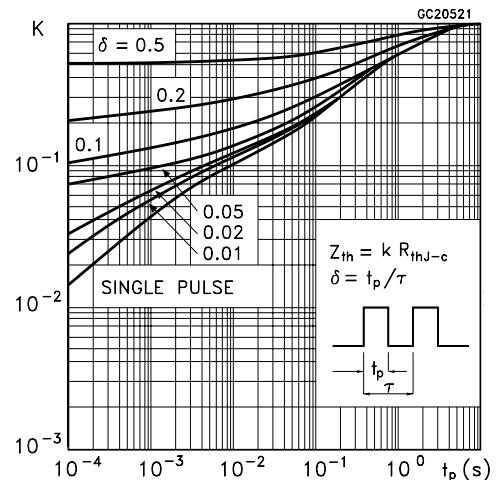


Figure 8: Transfer Characteristics

