



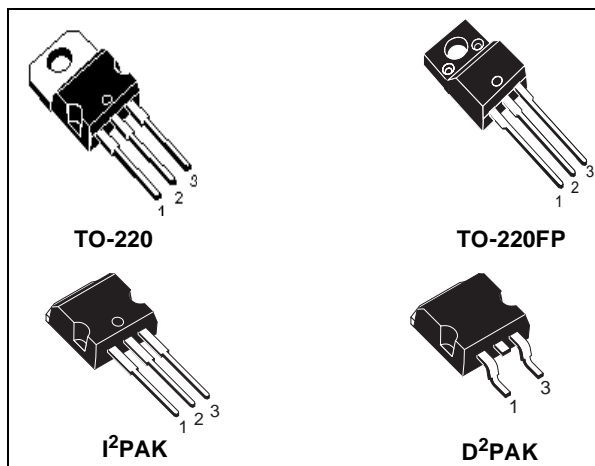
STP9NK60Z - STP9NK60ZFP STB9NK60Z - STB9NK60Z-1

N-CHANNEL 600V - 0.85Ω - 7A TO-220/FP/D²PAK/I²PAK

Zener-Protected SuperMESH™ Power MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STP9NK60Z	600 V	< 0.85 Ω	7 A	125 W
STP9NK60ZFP	600 V	< 0.85 Ω	7 A	30 W
STB9NK60Z	600 V	< 0.85 Ω	7 A	125 W
STB9NK60Z-1	600 V	< 0.85 Ω	7 A	125 W

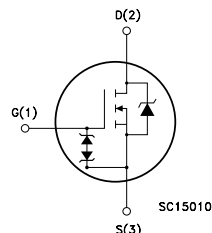
- TYPICAL R_{DS(on)} = 0.85 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- IMPROVED ESD CAPABILITY
- 100% AVALANCHE RATED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY



DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP9NK60Z	P9NK60Z	TO-220	TUBE
STP9NK60ZFP	P9NK60ZFP	TO-220FP	TUBE
STB9NK60Z	B9NK60Z	D ² PAK	TUBE
STB9NK60ZT4	B9NK60Z	D ² PAK	TAPE & REEL
STB9NK60Z-1	B9NK60Z-1	I ² PAK	TUBE

STP9NK60Z / STP9NK60ZFP / STB9NK60Z / STB9NK60Z-1**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value		Unit
		TO-220 / D ² PAK / I ² PAK	TO-220FP	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	600		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	600		V
V _{GS}	Gate- source Voltage	± 30		V
I _D	Drain Current (continuous) at T _C = 25°C	7	7 (*)	A
I _D	Drain Current (continuous) at T _C = 100°C	4.4	4.4 (*)	A
I _{DM} (•)	Drain Current (pulsed)	28	28 (*)	A
P _{TOT}	Total Dissipation at T _C = 25°C	125	30	W
	Derating Factor	1	0.24	W/°C
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	4000		V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5		V/ns
V _{ISO}	Insulation Withstand Voltage (DC)	-	2500	V
T _j	Operating Junction Temperature	-55 to 150		°C
T _{stg}	Storage Temperature	-55 to 150		°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤ 7A, di/dt ≤ 200 μA, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}.

(*) Limited only by maximum temperature allowed

THERMAL DATA

		TO-220 I ² PAK	D ² PAK	TO-220FP	
R _{thj-case}	Thermal Resistance Junction-case Max	1		4.16	°C/W
R _{thj-pcb}	Thermal Resistance Junction-pcb Max (When mounted on minimum Footprint)		30		°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	62.5			°C/W
T _I	Maximum Lead Temperature For Soldering Purpose	300			°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	7	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	235	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	I _{gs} =± 1mA (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

STP9NK60Z / STP9NK60ZFP / STB9NK60Z / STB9NK60Z-1

ELECTRICAL CHARACTERISTICS (TCASE = 25°C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 100\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 3.5 \text{ A}$		0.85	0.95	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15 \text{ V}$, $I_D = 3.5 \text{ A}$		5.3		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$		1110 135 30		pF pF pF
$C_{oss \text{ eq.}} (3)$	Equivalent Output Capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V to } 480 \text{ V}$		72		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 300 \text{ V}$, $I_D = 3.5 \text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3)		19 17		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 480 \text{ V}$, $I_D = 7 \text{ A}$, $V_{GS} = 10\text{V}$		38 7 21	53	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 300 \text{ V}$, $I_D = 3.5 \text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3)		43 15		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 300 \text{ V}$, $I_D = 7 \text{ A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (Inductive Load see, Figure 5)		11 8 20		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				7 28	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 7 \text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 7 \text{ A}$, $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 30\text{V}$, $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		480 3.5 14.5		ns μC A

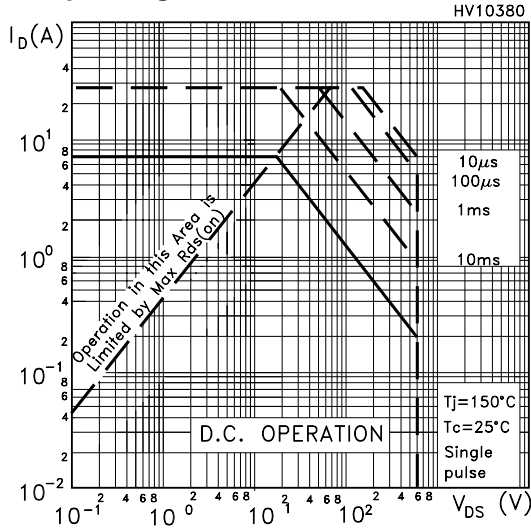
Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

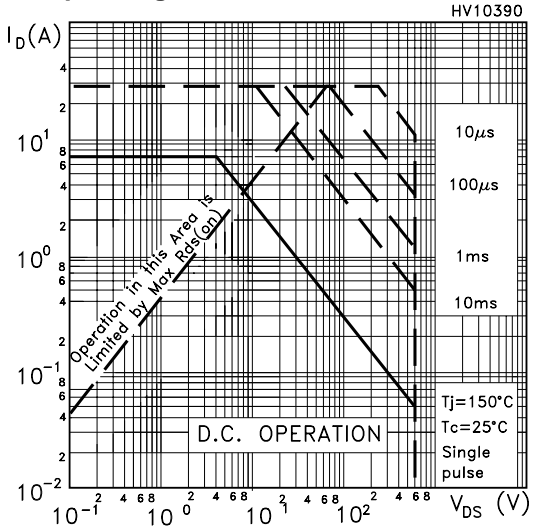
3. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

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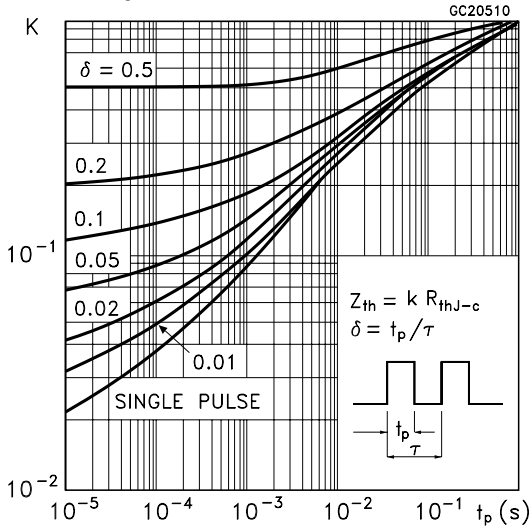
Safe Operating Area For TO-220/D2PAK/I2PAK



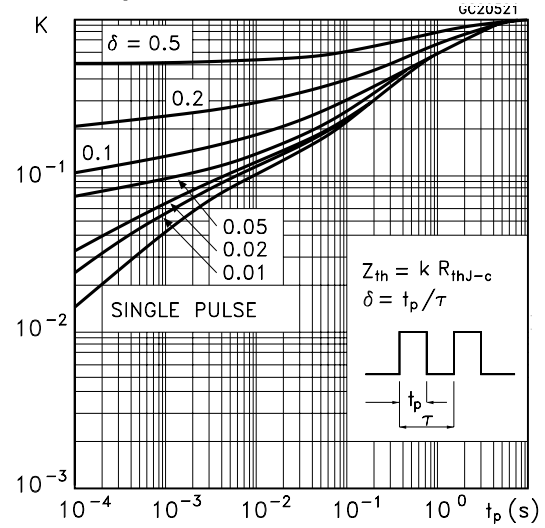
Safe Operating Area For TO-220FP



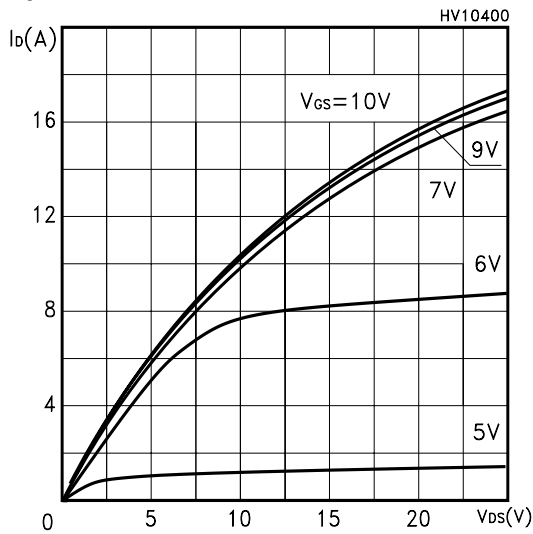
Thermal Impedance For TO-220/D2PAK/I2PAK



Thermal Impedance For TO-220FP



Output Characteristics



Transfer Characteristics

