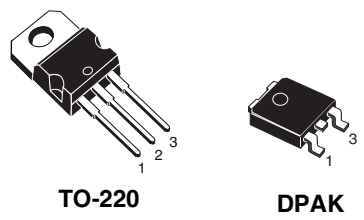
STD95N4F3
STP95N4F3

N-channel 40 V, 5.0 mΩ, 80 A, DPAK, TO-220
STripFET™ III Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	Pw
STD95N4F3	40 V	< 5.8 m Ω	80 A	110 W
STP95N4F3	40 V	< 6.2 mΩ	80 A	110 W

- Standard threshold drive
- 100% avalanche tested



Applications

- Switching applications
  - Automotive

Description

This STripFET™ III Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance providing superior switching performance.

Figure 1. Internal schematic diagram

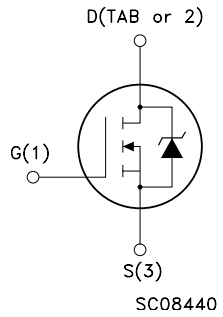


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD95N4F3	95N4F3	DPAK	Tape and reel
STP95N4F3	95N4F3	TO-220	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS}=0)	40	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	80	A
I_D	Drain current (continuous) at T_C = 100 °C	65	A
I_{DM} (2)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25 °C	110	W
	Derating factor	0.73	W/°C
dv/dt (3)	Peak diode recovery voltage slope	8	V/ns
E_{AS} (4)	Single pulse avalanche energy	400	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Current limited by package
2. Pulse width limited by safe operating area
3. $I_{SD} \leq$ 80 A, di/dt $\leq$ 400A/µs, $V_{DS} \leq V_{(BR)DSS}$, Tj $\leq$ Tjmax
4. Starting Tj = 25 °C, I_D = 40 A, V_{DD} = 30 V

Table 3. Thermal resistance

Symbol	Parameter	Value		Unit
		TO-220	DPAK	
$R_{thj-case}$	Thermal resistance junction-case max	1.36		°C/W
R_{thj-a}	Thermal resistance junction-ambient max	62.5		°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-ambient max		50	°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

1. When mounted on 1inch² FR-4 2Oz Cu board

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	40			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating,Tc = 125 °C			10 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 40 A for DPAK		5.0	5.8	mΩ
		V_{GS}= 10 V, I_D= 40 A for TO-220		5.4	6.2	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 25 V, I_D=40 A	-	100		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	2200 580 40		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=20 V, I_D = 80 A V_{GS} =10 V	-	40 11 8	54	nC nC nC

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}=20 V, I_D= 40 A, R_G=4.7 Ω, V_{GS}=10 V	-	15 50	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}=20 V, I_D= 40 A, R_G=4.7 Ω, V_{GS}=10 V	-	40 15	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		80 320	A A
V_{SD} (2)	Forward on voltage	I_{SD}=80 A, V_{GS}=0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=80 A, di/dt = 100 A/µs, V_{DD}= 30 V, Tj=150 °C	-	45 60 2.8		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

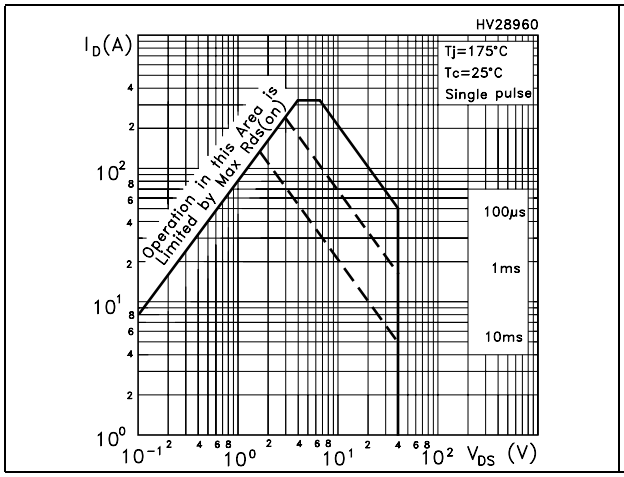


Figure 3. Thermal impedance

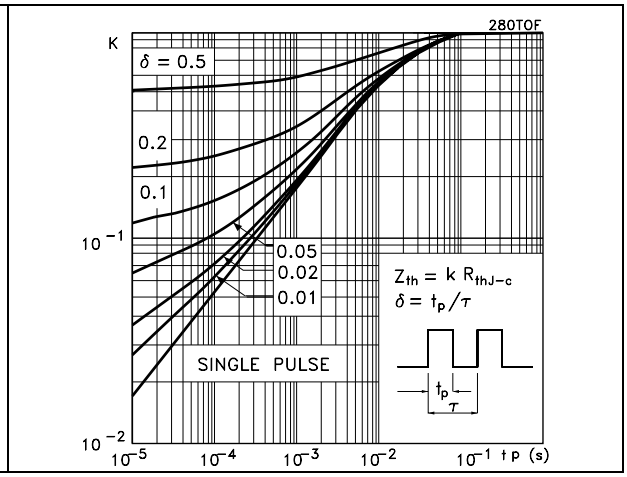


Figure 4. Output characteristics

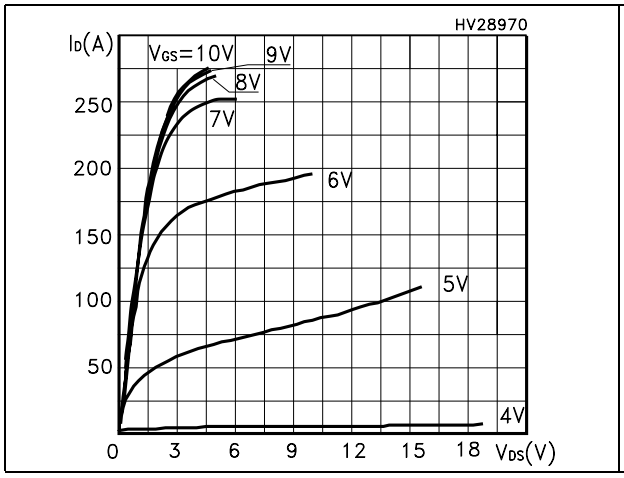


Figure 5. Transfer characteristics

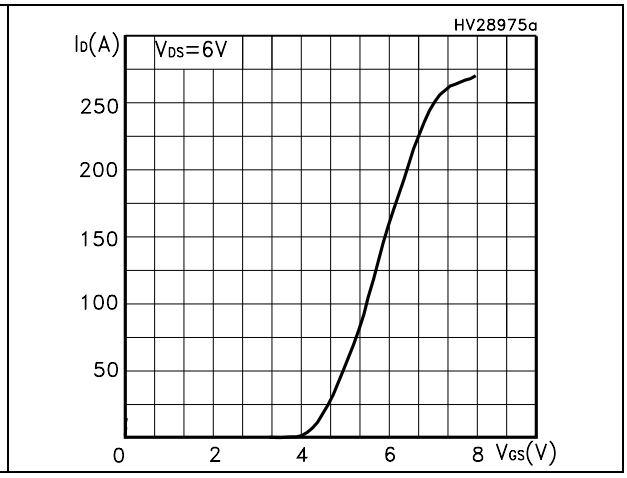


Figure 6. Static drain-source on resistance

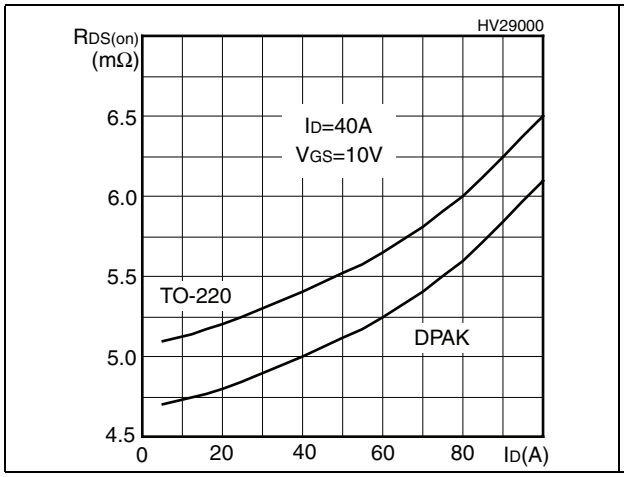


Figure 7. Normalized BVDSS vs temperature