STx8NM60N

N-channel 600 V, 0.56 Ω,7 A MDmesh™ II Power MOSFET TO-220, TO-220FP, IPAK, DPAK, D^{2}PAK

Features

Type	V_{DSS} (@Tjmax)	$R_{DS(on)}$ max	I_D
STB8NM60N	650 V	< 0.65 Ω	7 A
STD8NM60N	650 V	< 0.65 Ω	7 A
STD8NM60N-1	650 V	< 0.65 Ω	7 A
STF8NM60N	650 V	< 0.65 Ω	7 A(1)
STP8NM60N	650 V	< 0.65 Ω	7 A

1. Limited only by maximum temperature allowed

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

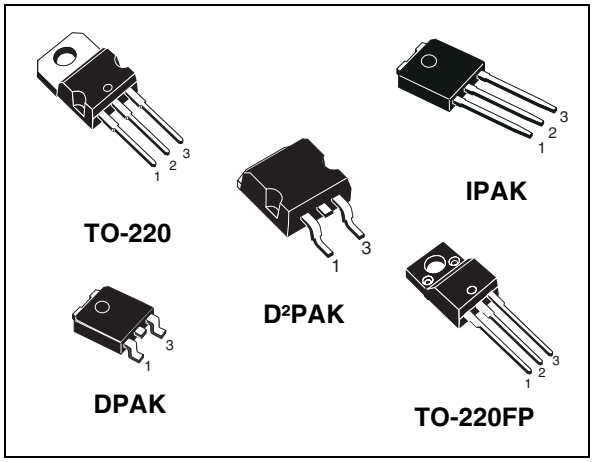
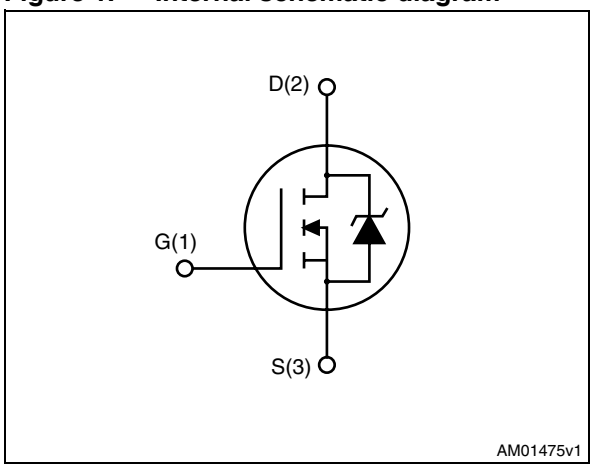


Figure 1. Internal schematic diagram



Application

- Switching applications

Description

This series of devices implements second generation MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the Company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB8NM60N	B8NM60N	D²PAK	Tape and reel
STD8NM60N	D8NM60N	DPAK	Tape and reel
STD8NM60N-1	D8NM60N	IPAK	Tube
STF8NM60N	F8NM60N	TO-220FP	Tube
STP8NM60N	P8NM60N	TO-220	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, IPAK, DPAK, D²PAK	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	600		V
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at T_C = 25 °C	7	7 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	4.3	4.3 (1)	A
I_{DM} (2)	Drain current (pulsed)	28	28 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	70	25	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s;T_C = 25 °C)	--	2500	V
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 7$ A, di/dt $\leq$ 400 A/µs, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value					Unit
		TO-220	IPAK	DPAK	D²PAK	TO-220FP	
Rthj-case	Thermal resistance junction-case	1.78				5	°C/W
Rthj-amb	Thermal resistance junction-amb	62.5	100	--	62.5		°C/W
T_l	Maximum lead temperature for soldering purpose	300					°C

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max)	2.5	A
E_{AS}	Single pulse avalanche energy (starting Tj = 25 °C, I_D = I_{AS}, V_{DD} = 50 V)	200	mJ

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
dv/dt(1)	Drain-source voltage slope	V_{DD} = 480 V, I_D = 7 A, V_{GS} =10 V		38		V/ns
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating,Tc = 125 °C			1 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 3.5 A		0.56	0.65	Ω

1. Characteristics value at turn off on inductive load

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}(1)	Forward transconductance	V_{DS} = 15 V, I_D= 3.5 A		15		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0		560 37 2		pF pF pF
$C_{oss\ eq.}$(2)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V		153		pF
R_G	Gate input resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		6		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 480 V, I_D = 7 A V_{GS} = 10 V		19 3 10		nC nC nC

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 300 V, I_D = 3.5 A, R_G = 4.7 Ω, V_{GS} = 10 V		10 12 40 10		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				7 28	A A
V_{SD}(2)	Forward on voltage	I_{SD} = 7 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 7 A, di/dt = 100 A/µs, V_{DD} = 30 V, Tj = 25 °C		310 2.40 15		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 7A, di/dt = 100 A/µs, V_{DD} = 30 V, Tj=150°C		480 3.50 15		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D²PAK

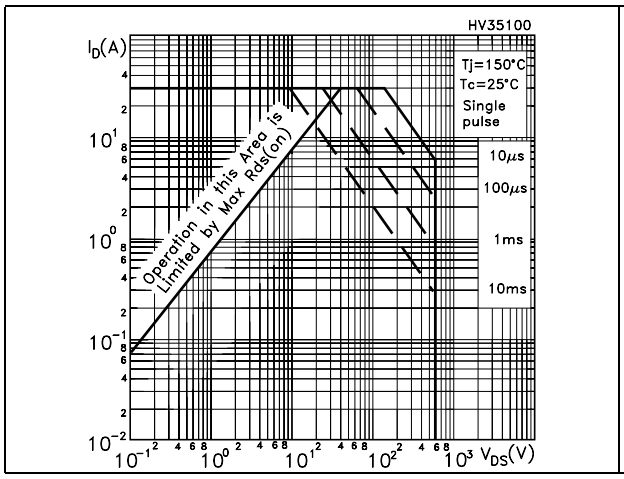


Figure 3. Thermal impedance for TO-220, D²PAK

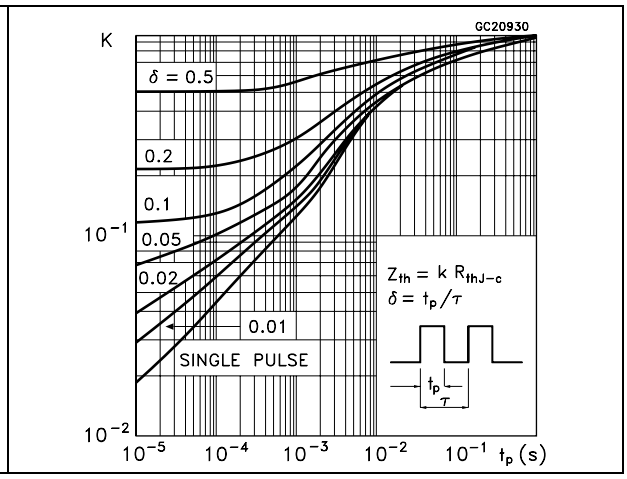


Figure 4. Safe operating area for DPAK, IPAK

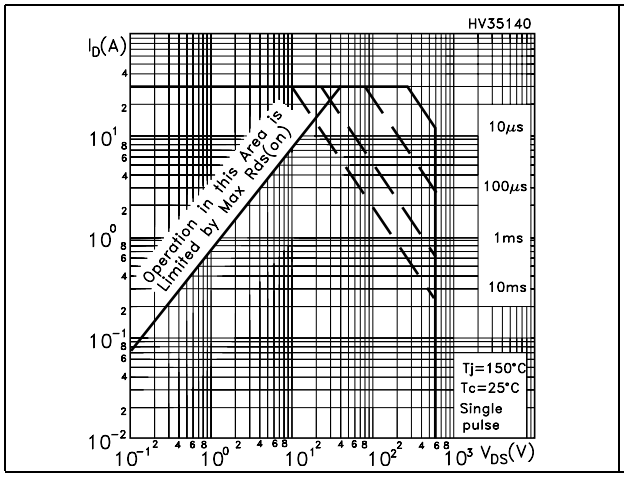


Figure 5. Thermal impedance for DPAK, IPAK

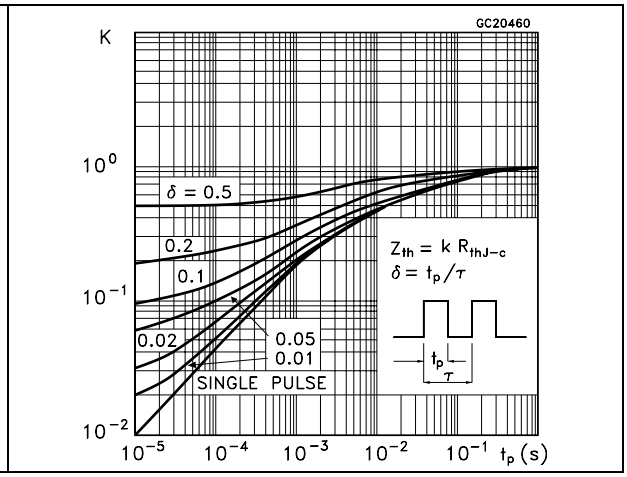


Figure 6. Safe operating area for TO-220FP

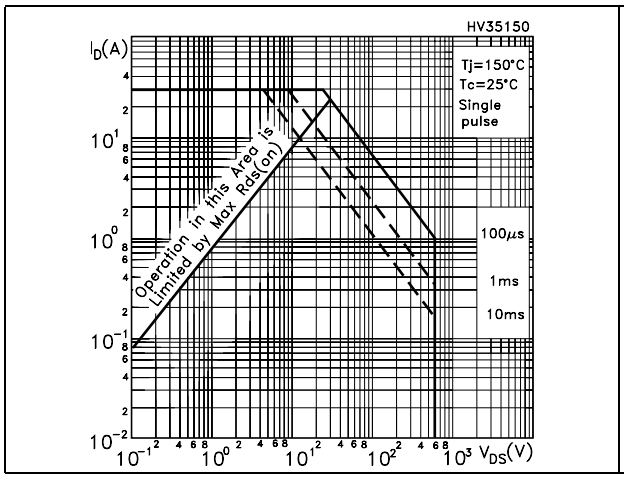


Figure 7. Thermal impedance for TO-220FP