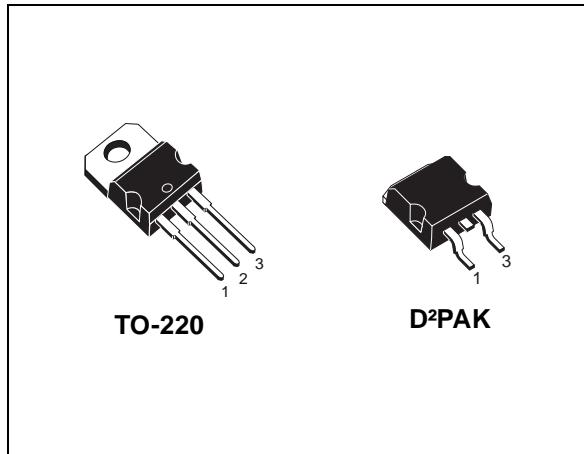


General features

Type	V _{DSS}	R _{DS(on)}	I _D	P _{TOT}
STB8NM60D	600V	< 1.0Ω	8A	100W
STP8NM60D	600V	< 1.0Ω	8A	100W

- High dv/dt and avalanche capabilities
- 100% avalanche rated
- Low input capacitance and gate charge
- Low gate input resistance
- Fast internal recovery diode



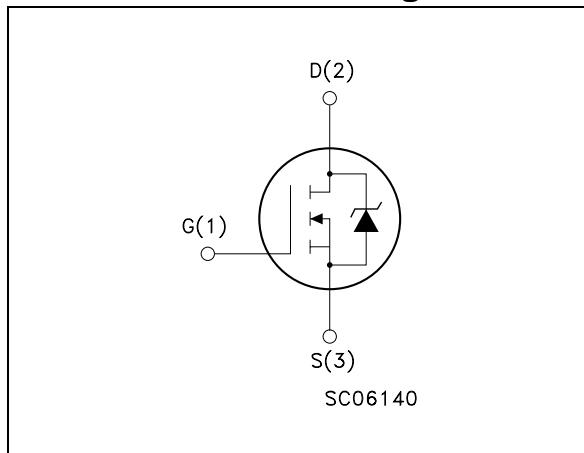
Description

The FDmesh™ associates all advantages of reduced on-resistance and fast switching with an intrinsic fast-recovery body diode. It is therefore strongly recommended for bridge topologies, in particular ZVS phase-shift converters

Applications

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.

Internal schematic diagram



Order codes

Sales Type	Marking	Package	Packaging
STB8NM60D	B8NM60D	D ² PAK	TAPE & REEL
STP8NM60D	P8NM60D	TO-220	TUBE

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS} = 0$)	600	V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20\text{k}\Omega$)	600	V
V_{GS}	Gate-Source Voltage	± 30	V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	8	A
I_D	Drain Current (continuous) at $T_C=100^\circ\text{C}$	5	A
$I_{DM}^{(1)}$	Drain Current (pulsed)	32	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	100	W
	Derating Factor	0.8	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak Diode Recovery voltage slope	20	V/ns
T_J	Operating Junction Temperature		
T_{stg}	Storage Temperature	-65 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2. $|I_{SD}| \leq 5\text{A}$, $di/dt \leq 400\text{A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$ **Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case Max	1.25	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$
T_I	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	2.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25^\circ\text{C}$, $I_D=I_{AR}$, $V_{DD}=50\text{V}$)	200	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0$	600			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$, $V_{DS} = \text{Max Rating}, T_c=125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate Body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 30\text{V}, V_{DS} = 0$			± 100	nA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	3	4	5	V
$R_{DS(\text{on})}$	Static Drain-Source On Resistance	$V_{GS} = 10\text{V}, I_D = 2.5\text{A}$		0.9	1	Ω

Table 5. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward Transconductance	$V_{DS} = I_{D(\text{on})} \times R_{DS(\text{on})\text{max}}$ $I_D = 2.5\text{A}$		2.4		s
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{V}, f = 1 \text{ MHz}, V_{GS} = 0$	380 170 14			pF pF pF
$C_{oss \text{ eq.}}^{(2)}$	Equivalent Output Capacitance	$V_{GS} = 0, V_{DS} = 0\text{V to } 480\text{V}$		60		pF
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 400\text{V}, I_D = 5\text{A}$ $V_{GS} = 10\text{V}$ (see Figure 13)	15 4 8	18		nC nC nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%
2. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=300V$, $I_D=2.5A$, $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 12)	13 10 26 8	ns ns ns ns	ns ns ns ns	ns ns ns ns
t_r	Rise Time					
$t_{d(off)}$	Turn-off Delay Time					
t_f	Fall Time					
$t_{d(off)}$	Turn-off Delay Time	$V_{DD}=480V$, $I_D=5A$, $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 12)	8 8 14	ns ns ns	ns ns ns	ns ns ns
t_f	Fall Time					
t_c	Cross-over Time					

Table 7. Source drain diode

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit				
I_{SD}	Source-drain Current				5	A				
$I_{SDM}^{(1)}$	Source-drain Current (pulsed)				20	A				
$V_{SD}^{(2)}$	Forward on Voltage	$I_{SD}=5A$, $V_{GS}=0$		1.5	V					
t_{rr}	Reverse Recovery Time	$I_{SD}=5A$, $dI/dt = 100A/\mu s$, $V_{DD}=50 V$, $T_j=25^\circ C$								
Q_{rr}	Reverse Recovery Charge									
I_{RRM}	Reverse Recovery Current									
t_{rr}	Reverse Recovery Time	$I_{SD}=5A$, $dI/dt = 100A/\mu s$, $V_{DD}=50 V$, $T_j=150^\circ C$		178	ns	ns				
Q_{rr}	Reverse Recovery Charge									
I_{RRM}	Reverse Recovery Current									

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300μs, duty cycle 1.5%