STB85NF55L
STP85NF55L

N-channel 55 V, 0.0060 Ω, 80 A, TO-220, D^{2}PAK
STripFET™ II Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STB85NF55L	55 V	< 0.008 Ω	80 A
STP85NF55L	55 V	< 0.008 Ω	80 A

- Low threshold drive

Application

- Switching applications

Description

This Power MOSFET is the latest development of STMicroelectronis unique "single feature size" strip-based process. The resulting transistorshows extremely high packing density for low on-resistance, rugged avalanche characteristics andless critical alignment steps therefore a remarkable manufacturing reproducibility.

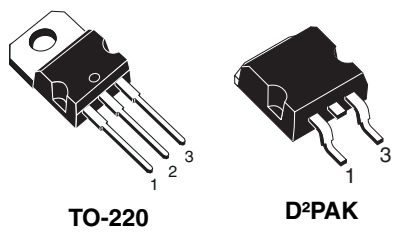

Figure 1. Internal schematic diagram

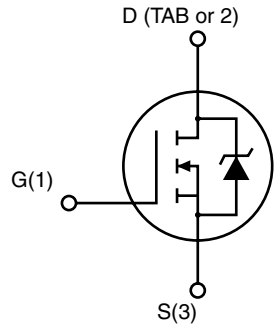

Table 1. Device summary

Order code	Marking	Package	Packaging
STB85NF55LT4	B85NF55L	D²PAK	Tape and reel
STP85NF55L	P85NF55L	TO-220	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	55	V
V_{GS}	Gate-source voltage	± 15	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	80	A
I_D(1)	Drain current (continuous) at T_C=100 °C	80	A
I_{DM}(2)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25 °C	300	W
	Derating factor	2.0	W/°C
dv/dt (3)	Peak diode recovery voltage slope	10	V/ns
E_{AS} (4)	Single pulse avalanche energy	980	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Current limited by package
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 80$ A, di/dt ≤ 300 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
4. Starting T_J = 25 °C, I_D = 40 A, V_{DD} = 40 V

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		D^2PAK	TO-220	
$R_{thj-case}$	Thermal resistance junction-case max.	0.5		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max.	62.5		°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max.(1)	35		°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

1. When mounted on 1inch² FR-4 2Oz Cu board

2 Electrical characteristics

(T_{CASE}= 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	55			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating, V_{DS} = max rating @125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±15 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1	1.6	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 40 A		0.0060	0.008	Ω
		V_{GS}= 5 V, I_D= 40 A		0.008	0.01	

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 40 A	-	130		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f = 1 MHz, V_{GS} = 0	-	4050 860 300		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 27.5 V, I_D = 80 A V_{GS} = 5 V	-	80 20 45	110	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}= 27.5 V, I_D= 40 A, R_G=4.7 Ω, V_{GS}= 5 V	-	35 165 70 55	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		80	A
I_{SDM}(1)	Source-drain current (pulsed)		-		320	A
V_{SD}(2)	Forward on voltage	I_{SD} = 80 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 80 A, di/dt = 100 A/µs, V_{DD} = 20 V, T_J = 150 °C	-	80 240 6		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

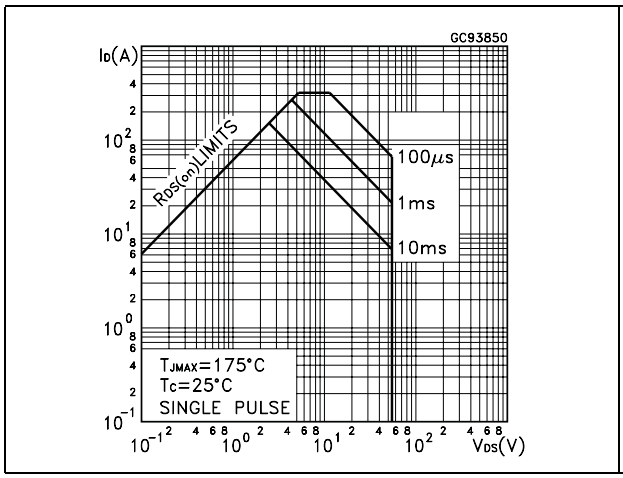

Figure 3. Thermal impedance

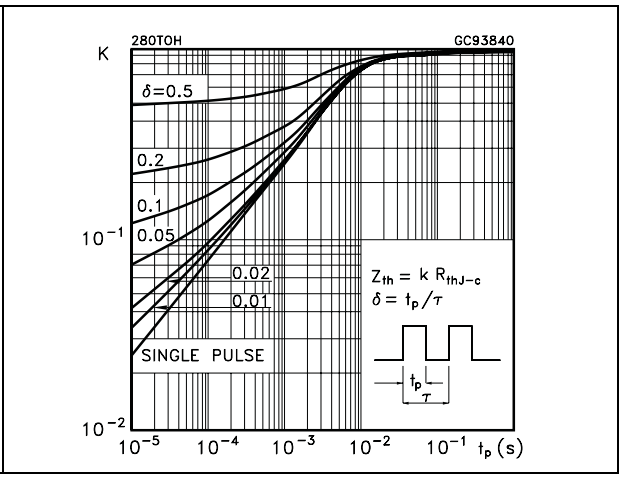

Figure 4. Output characteristics

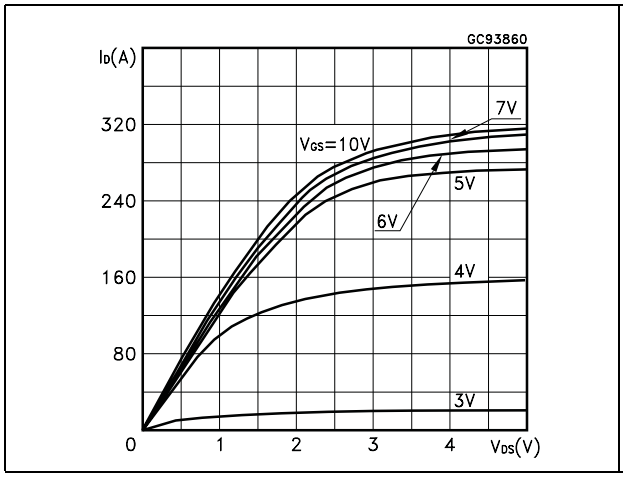

Figure 5. Transfer characteristics

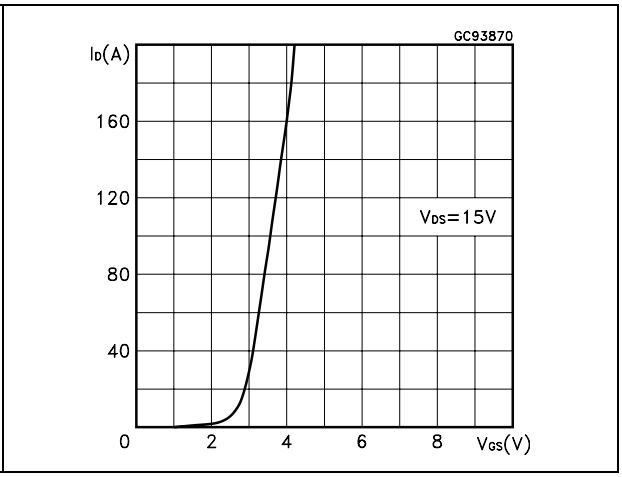

Figure 6. Transconductance

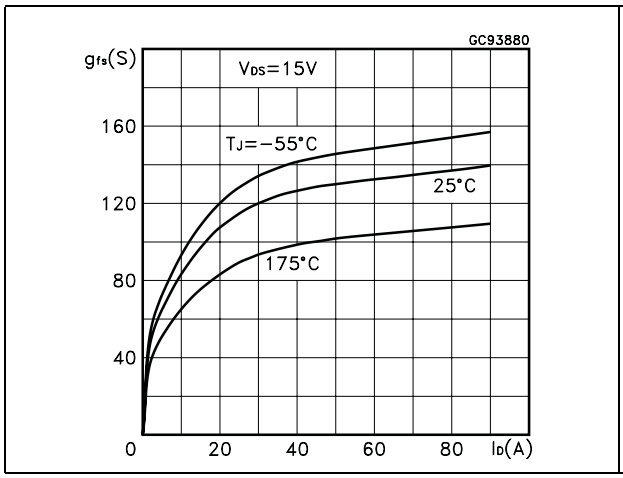

Figure 7. Static drain-source on resistance