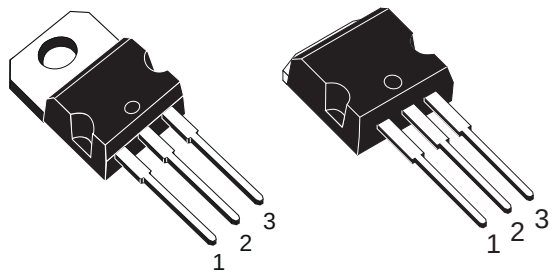
STP85NF3LL
STB85NF3LL-1

N-CHANNEL 30V - 0.006Ω - 85A TO-220/I^{2}PAK
LOW GATE CHARGE STripFET™ POWER MOSFET

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP85NF3LL	30 V	< 0.008 Ω	85 A
STB85NF3LL-1	30 V	< 0.008 Ω	85 A

- TYPICAL R_{DS}(on) = 0.0075 Ω (@4.5V)
- OPTIMAL $R_{DS(ON)}$ x Qg TRADE-OFF @4.5V
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED

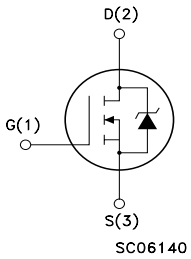


TO-220 **I^{2}PAK**

DESCRIPTION

This application specific Power MOSFET is the third genaration of STMicroelectronics unique " Single Feature Size" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	30	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	30	V
V_{GS}	Gate- source Voltage	± 15	V
I_D	Drain Current (continuos) at T_C = 25°C	85	A
I_D	Drain Current (continuos) at T_C = 100°C	60	A
I_{DM} (●)	Drain Current (pulsed)	340	A
P_{TOT}	Total Dissipation at T_C = 25°C	110	W
	Derating Factor	0.73	W/°C
T_{stg}	Storage Temperature	–65 to 175	°C
T_j	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1.36	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 15V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 40 A		0.006	0.008	Ω
		V_{GS} = 4.5V, I_D = 40 A		0.0075	0.0095	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 40 A		30		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		2210		pF
C_{oss}	Output Capacitance			635		pF
C_{rss}	Reverse Transfer Capacitance			138		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 15V, I_D = 30A R_G = 4.7Ω V_{GS} = 4.5V (see test circuit, Figure 3)		22 130		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 24V, I_D = 60A, V_{GS} = 4.5V		30 9 12.5	40	nC nC nC

SWITCHING OFF

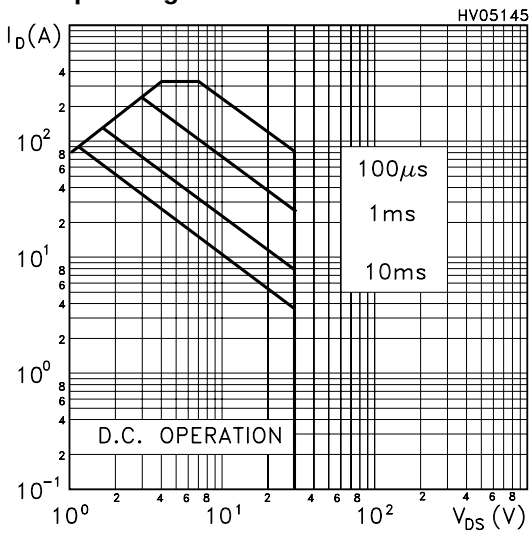
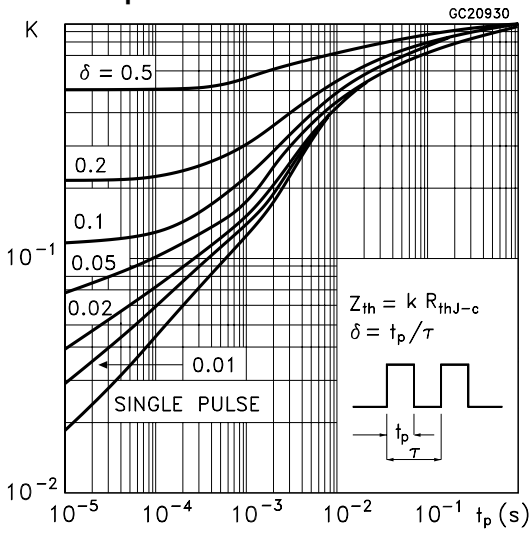
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off-Delay Time Fall Time	V_{DD} = 15V, I_D = 30A, R_G = 4.7Ω, V_{GS} = 4.5V (see test circuit, Figure 3)		36.5 36.5		ns ns
$t_{d(off)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	Vclamp =24V, I_D =30A R_G = 4.7Ω, V_{GS} = 4.5V (see test circuit, Figure 5)		32 23 40		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain Current Source-drain Current (pulsed)				85 340	A A
V_{SD} (2)	Forward On Voltage	I_{SD} = 85A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 85A, di/dt = 100A/µs, V_{DD} = 15V, T_j = 150°C (see test circuit, Figure 5)		65 105 3.4		ns nC A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Safe Operating Area



Thermal Impedence